

Sustaining Standards Leadership

The United States Cannot Disengage from RISC-V

By Sujai Shivakumar and Julie Heng

RISC-V architecture is an open, international standard governing how software interfaces with hardware in a computer. It serves as a shared language that sets the parameters for communication and interoperability. Open standards provide a means for industry participants to collaborate and develop technological solutions that can help accelerate innovation and limit misuse of intellectual property (IP).

Some policymakers fear an open standard could threaten U.S. national security and competitive advantage. However, the openness of the standard does not by itself pose a risk. Indeed, RISC-V does not contain sensitive IP, nor does its cooperative development require firms to divulge IP. Firms compete on technologies developed using this platform, not on the platform itself. RISC-V enhances the competitiveness of U.S. chip design firms by creating a flexible, low-risk, and low-cost platform for collaboration. To capitalize on this opportunity, the United States should continue to support RISC-V for future chip innovation.

RISC-V in the ISA Landscape

Currently, there are two leading semiconductor **instruction set architectures (ISAs)** covering most of the market: x86 (from U.S.-based Intel/AMD) and ARM (from United Kingdom-based Arm Holdings, which is majority owned by the Japanese SoftBank Group). There are two primary kinds of ISAs—complex instruction set computers (CISCs) and reduced instruction set computers (RISCs)—which are organized differently and operate at different **efficiencies**; x86 is based on CISC principles, and ARM is based on RISC. x86 ISAs are used in most laptop and desktop computers, while ARM has almost complete market share in the mobile world. ARM and Intel/AMD ISAs are proprietary standards, so other companies and designers can license ARM IP or buy and use processors based on Intel/AMD IP.

Table 1: Leading Instruction Set Architectures by Type and Kind of Standard

Kind of Standard	Type of Architecture	
	CISC	RISC
	Proprietary	x86 (from Intel/AMD) ARM (from Arm Holdings)
	Open	RISC-V (industry standard)

By contrast, the newest entrant to the field is RISC-V (pronounced “risk five”), an open-standard ISA based on RISC principles that chip design teams can access and implement for free across various use cases without restrictions on licensing. In other words, RISC-V allows for easy customization with a royalty-free license and no license restrictions on modifications.

A Global Platform: Initially **developed** at the University of California, Berkeley’s Parallel Computing Laboratory **in 2010**, RISC-V is now managed by the Swiss nonprofit standards body **RISC-V International**. The nonprofit attracts a diverse community of 4,600 members across 70 countries, and includes firms, universities, community organizations, and individuals who collaboratively develop the RISC-V ISA and its extensions. RISC-V International’s Technical Steering Committee includes U.S. entities (e.g., Google and Qualcomm), as well as Chinese organizations (e.g., Alibaba and Huawei). Of RISC-V International’s 24 premier members, which span startups to VC firms to hyperscalers, 12 are based in China, 9 in the United States, and 1 each in Taiwan, Brazil, and Spain. The board and overall membership composition is split among the United States, China, and Europe, with the United States slightly leading in numbers.

Flexibility and Accessibility: RISC-V’s flexibility and accessibility make it an attractive ISA with growing momentum. Early use cases are in the **embedded system** market, with potential applications in high-performance computing (HPC) and artificial intelligence (AI), as well as consumer electronics and wearables. There are currently over 2 billion RISC-V-based chips, a number that is **projected** to grow to 20 billion by 2031. RISC-V International, which has **grown** in membership from 236 members in 2019 to over 4,600 in 2025, seeks to capitalize on this support. In late 2019, escalating geopolitical tensions prompted the RISC-V International governing body to move from Delaware to Switzerland, **citing** its mission to ensure that universities, governments, and companies outside the United States could access and develop its technology. Since then, the nonprofit has been building out tools and opportunities for collaboration in the ecosystem, with 68 new specifications and over 80 working groups.

A Low-Cost, High-Control Platform: Many firms that currently buy x86 or license ARM ISAs are helping to develop RISC-V so that they can have another option for semiconductor architectures without incurring expensive licensing fees. This allows engineers to build their own implementations on top of the ISA, enabling them to maintain greater control over their technology and take advantage of software compatibility across the RISC-V ecosystem. For example, Nvidia **began** transitioning away from its proprietary microcontrollers to RISC-V-based cores in 2015, just five years after the

open-standard ISA was introduced. Other industry giants such as Google, Qualcomm, and Samsung have made similar moves. A customizable, low-cost ISA option is also attractive for smaller firms.

A Secure IP Environment: It is important to note again that RISC-V does not contain sensitive IP, nor does its cooperative development require firms to divulge such IP. RISC-V standard-setting **does not require** U.S. firms to share confidential information with other firms. Corporations' sensitive IP is only used in their implementation of RISC-V, not shared through the RISC-V platform itself, and firms can license their RISC-V implementation. Startups like SiFive and Tenstorrent, for example, use the RISC-V ISA and then license their implementations of it as IP. Furthermore, some argue that open-source ISA designs are more secure than closed designs because they allow members of the technical community to locate vulnerabilities collectively.

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The Business Case for RISC-V

Rapid Industry Adoption: According to BCC Publishing, market revenue for RISC-V technology is projected to grow at a compound annual growth rate of **33.1 percent from 2022 to 2027**. The Defense Advanced Research Projects Agency (DARPA) **supported** RISC-V multicore processor development in 2018. As of 2025, many U.S. firms are rapidly investing in RISC-V-based software implementations, from microcontrollers in GPUs from Nvidia to 5G mmWave RF in Samsung and HDD controllers in Seagate. Indeed, in May 2023, industry leaders and startups cooperatively launched the **RISC-V Software Ecosystem (RISE) Project**, which intends to expedite the incorporation of RISC-V software into consumer electronics, data centers, and automotive products. RISE's 13 premier members and 10 general members include Google, Intel, Nvidia, Qualcomm, Red Hat, Rivos, SiFive, Ventana, Samsung, Mediatek, Bytedance, and Tenstorrent.

Large industry players have also publicly described the expanding role of RISC-V architecture in AI applications and scaling. In 2018, Google helped found OpenTitan with the aim of developing an open-source, root-of-trust chip, which has been enabled by community members and partners in industry and academia. Qualcomm uses RISC-V cores in some of its Snapdragon processors and has shipped over 650 million such cores in its devices. Nvidia revealed in October 2024 that its custom CUDA cores rely on the RISC-V ISA standard. The company has developed at least three RISC-V microcontroller cores so far and, as of October 2024, expected to ship a billion across its products.

Greater Technical Flexibility: Why are so many firms investing in RISC-V? The answer comes down to flexibility and cost, primarily in terms of supply chain and customizability. Licensing requirements are expensive and limiting, not to mention legally complicated. Furthermore, RISC-V is currently

more flexible on the technical side than earlier ISAs. x86, for example, has been iterated upon for a long time, accruing extensions and complications, making it **hard to work with** for new applications. RISC-V-based cores do not have legacy issues from prior generations, and they can be more easily tailored for performance benefits or higher computation densities. As a spokesperson for Ventana Micro **explained**, “Addition of an instruction in RISC-V is a relatively straightforward process of coming up with an instruction definition, providing the needed justification for the instruction and driving it through the RISC-V International Technical Steering Committee.”

While the recent growth of RISC-V offers advantages, its newness also means that it does not have the same technical and customer support network as proprietary ISAs. While ARM’s proprietary technology comes with support and liability coverage, RISC-V International is currently trying to build up that ecosystem. As a spokesperson for Ventana Micro **explained**, “The goal is always to drive all new instructions/extensions through RISC-V International to prevent fragmentation in the industry. That said, you can always quickly blaze ahead to incubate an acceleration idea on top of the common base if you really need to get something done. That is what is bringing a lot of AI applications to RISC-V.”

Growing Adoption of RISC-V

RISC-V is not just a competitor to x86 and ARM but rather represents a breakthrough alternative in chip design for a wide range of current and potential applications.

Current Applications: So far, RISC-V has been adopted **mostly** in embedded tech, with market possibilities in the wearable, global automotive, and HPC/AI industries on the horizon. Chips from the fabless company SiFive, an early proponent of RISC-V high-performance chips, **are found in** Google data centers and NASA’s High-Performance Spaceflight Computer. RISC-V has also been tapped to **build flexible chips** that could power wearable healthcare electronics, smart package labels, soft robotics, and other inexpensive items.

Future Applications: While RISC-V won’t be competitive with x86 and ARM in mainstream consumer electronics applications for at least 10 years, leading firms are already using RISC-V to develop future capabilities. Alibaba is developing RISC-V chips for edge computing, and Hong Kong-based DeepComputing has released the world’s first RISC-V laptops, though their performance currently lags **behind** that of laptops using proprietary ISA counterparts. In 2024, engineers from Intel’s Advanced Architecture Development Group **established** AheadComputing Inc., a startup focused on developing RISC-V core IP.

Need for Infrastructure: Crucially, for RISC-V to become a major force in mainstream devices, there needs to be a robust ecosystem of tools, support systems, and resources built to attract chipmakers and manufacturers. One key sign of progress was RISC-V International’s October 2024 ratification of the RVA23 profile, a standardized set of ISA extensions compatible with RISC-V, though much remains to be done to support its development ecosystem.

The International RISC-V Landscape

THE UNITED STATES

Currently, the United States is the leader in chip design, meaning that U.S.-designed chips lead the global market in performance, energy efficiency, sophistication, and market share. The emergence

of RISC-V—as an alternative platform that allows all countries, firms, and individuals to design chip architectures—raises concerns about the ability of U.S. firms to sustain this leadership.

Enabling China’s Progress? In late 2023, **some members of Congress** expressed concern over the national security implications of Chinese firms’ involvement in developing RISC-V. These policymakers worry that Chinese firms will use the RISC-V architecture to bypass U.S. export controls, potentially using RISC-V in high-performance chips in the future. Those who urge caution point out that open-source software helped enable the rise of Chinese companies like ByteDance and Tencent, and that RISC-V could similarly aid Chinese firms in the hardware space. In this regard, Serge Leef, a DARPA microcontroller product manager, has **argued** that it is “not unlikely” that RISC-V could be “giving China a leg up on all these technologies because they can now save 20 years of engineering and catch up to Western technology overnight.” In response to such concerns, the Department of Commerce **announced** in April 2024 that it was reviewing the national security implications of RISC-V.

Excluding U.S. firms from the standards process would likely not stop global development, however, which means U.S. firms would be forced to develop technologies that fit different ISAs, license expensive proprietary standards, or adopt less efficient technologies.

Or an Opportunity for U.S. Innovation? In contrast, major semiconductor firms see RISC-V as a significant opportunity for innovation. Many are considering basing future designs on RISC-V, reducing dependence on ARM, and expanding their markets. For example, last year, Business Korea **reported** that Samsung Electronics established an Advanced Processor Lab in Silicon Valley dedicated to RISC-V-based AI chip design.

Limited Options: Whatever concerns some U.S. policymakers may have, regulatory options over RISC-V are limited because RISC-V International operates outside the United States. In fact, the organization moved overseas to avoid potential breaches of U.S. sanctions against Huawei and other Chinese companies, which are RISC-V members. This means that the United States cannot restrict the publication of RISC-V standards or determine which other countries participate in the process. The only immediate, but not necessarily effective, option would be to restrict U.S. firms from participating in RISC-V standards development. Excluding U.S. firms from the standards process would likely not stop global development, however, which means U.S. firms would be forced to develop technologies that fit different ISAs, license expensive proprietary standards, or adopt less efficient technologies.

CHINA

In **seeking** greater technological autonomy and self-sufficiency, China is looking to RISC-V as an alternative to licensing IP blocks from Western firms such as Intel and Arm. As one Chinese media article **puts** it (translated by the authors), “You cannot build a house on someone else’s foundation.”

Reflecting a longstanding commitment to reducing dependence on U.S. technology, the Chinese government is incentivizing the use of RISC-V architecture in chip design, primarily among firms based in Beijing, **Shanghai**, and **Shenzhen**, and more recently in **Wuhan**. For example:

- The RISC-V Industry Alliance convened local startups in a collaboration that had grown to 173 companies by mid-2023.
- In 2023, nine leading chip design firms, including Alibaba’s chip unit (T-Head) and Baidu-backed StarFive, formed a patent alliance for RISC-V to enable the sharing of IP and licensing to third parties to promote a “healthy” (i.e., Chinese centric) open-source environment and the “rapid development” of RISC-V technologies.
- In 2023, Alibaba’s chip design subsidiary, T-Head, launched a RISC-V-based controller chip, Zhenyue 510, for applications in artificial intelligence training, online transactions, and big data analysis. A T-Head executive **said** that his company was launching an initiative to encourage 150,000 developers to learn about and secure international credentials with respect to RISC-V.
- The Beijing Open-Source Chip Research Institute, a group of research centers that includes members from the Chinese Academy of Sciences and hyper-scalers Tencent and Alibaba, is developing indigenous chip design architecture based on RISC-V. Scientists at the academy **released** a RISC-V-based processor called XiangShan and **aim** to produce a commercial version in 2025.
- Alibaba’s research arm, Damo Academy, launched the next generation of its RISC-V XuanTie processors for applications in 5G communications, robotics, and financial services in February 2025.
- China has **invested** heavily and incentivized engagement in standards-setting processes, seeking to exert more influence over the development and use of technology standards—raising important questions about its impact on the broader networks of innovation, competition, trade, and security. Reflecting its strong endorsement, in March 2025, there were **reports** that China plans to issue guidance to encourage RISC-V chip use.

EUROPE

According to the European Strategy and Policy Analysis System, the European Union’s share of global chip revenue **dropped from about 20 percent** in the 1990s to less than 10 percent in the 2020s. The **European Processor Initiative** (EPI), launched with European Commission and, later, **European Chips Act** support, seeks to reduce Europe’s foreign-chip dependence and grow its own processor industry.

Even as these initiatives aim to reduce Europe’s reliance on U.S. and Asian suppliers for critical technologies, RISC-V has “opened the possibility for anyone in the world, including Europe, to make processors,” **according** to Mateo Valero, director of the Barcelona Supercomputing Cluster. Aiming to create a “Design Valley” in Spain, the Barcelona Supercomputing Cluster has worked on RISC-V technology since the 2010s. In 2023, the cluster **presented** Sargantana, the latest generation of open-source indigenous chips. Other smaller European firms using RISC-V include Gaisler, Esperanto Technologies, Semidynamics, and Codaip, with growing momentum in the embedded systems market. The Barcelona Supercomputing Cluster is also helping **coordinate** the new Digital Autonomy with

RISC-V in Europe (DARE) Project, which brings together 38 tech players to try and create three chiplets. The six-year project is backed by €240 million from the EuroHPC public-private partnership.

Some European stakeholders caution against unrealistic expectations of complete chip sovereignty and, as in China, call instead for strategic collaboration within the RISC-V framework. Indeed, the *EE Times* **reported** in early 2024 that Nordic Semiconductor, Bosch, NXP, Agile Analog, and Semidynamics are among the European semiconductor industry players contributing to the rise in RISC-V-centered collaborations to reduce dependencies on other firms: “the community is anxious not to repeat the mistakes made with Arm.”

NEW ENTRANTS ARE INVESTING IN RISC-V-BASED SYSTEMS DUE TO SPEED OF DEVELOPMENT AND LOWER COSTS

India: The Indian government is investing in developing a series of indigenous processors, with significant work **from** the Shakti program at IIT-Madras. National investment programs, such as the **Digital India RISC-V Program** in academia and industry, aim to **support** the development of a RISC-V-centered innovation hub in Bengaluru.

Brazil: The Brazil Ministry of Science, Technology, and Innovation is a premier member of RISC-V International. Institutions like the Eldorado Institute and the Wernher von Braun Advanced Research Center are focusing on RISC-V projects, **including** an international collaborative partnership with the Barcelona Supercomputing Center.

RISC-V as Strategic Opportunity for U.S. Standards Innovation Leadership

Given the rapid adoption of the RISC-V platform and its benefits for enhanced interoperability and collaboration, what are the options for U.S. policy? Recent analyses have highlighted RISC-V policy considerations for U.S. policymakers:

The Need for a Better Understanding of RISC-V: A 2024 **commentary** pointed out that RISC-V has not been well understood by policymakers—in particular the fact that chip competition occurs at the implementation level, not at the standards level. This means that each firm implements the ISA uniquely, adding their proprietary innovations independently. In short, RISC-V does not involve transfers of sensitive technology, and companies typically do not give away their IP during standards discussions—so, in principle, China’s participation in RISC-V does not grant access to advanced semiconductor technology.

The Importance of Continued Engagement with RISC-V: Efforts to force U.S. firms out of RISC-V would be dysfunctional in that they would not stop the use of RISC-V by Chinese and other firms but would in fact cede innovation to Chinese firms. Indeed, some U.S. firms would still need to use RISC-V but would lose influence over its development. This could lead to a fragmented RISC-V ecosystem, potentially disadvantaging U.S. firms that would have to develop multiple RISC-V systems without being able to influence the ecosystem’s trajectory. Moreover, there are good commercial and technical reasons for U.S., European, and other firms to support RISC-V. It enables them to avoid dependency on a single proprietary standard and to benefit from a low-cost, adaptable, widely adopted standard that continues to improve.

Constraints on Regulatory Approaches: A 2024 [CSET article](#) highlighted how U.S. regulatory options over RISC-V are limited because RISC-V is managed by a Swiss standards body; the only real possibility would be to restrict U.S. involvement in RISC-V standards. But such a move would be counterproductive for U.S. firms (which may leave the United States so that they can use RISC-V in other countries) and could harm U.S. tech leadership and competitiveness.

A major advantage of RISC-V is that it is a low-cost standard that can be leveraged by researchers, taught and used in universities, and adopted by small startups as well as large companies. . . . Importantly, RISC-V is a means to bring the innovative ideas of a new generation of researchers to the market.

The “**The Promise and Paranoia of RISC-V**” section of a 2021 Foreign Policy Research Institute report takes a longer-term view: RISC-V presents a lot of opportunities in terms of its adaptability and implementation, the report asserts, and the United States must invest in RISC-V at home to ensure that it is positioned to lead the field of open-source hardware. The report notes that though some fear the rise of this new standard, the United States has much to gain from it. While RISC-V would lower the price of chip design and lead to commoditization in some areas of the chip industry, it would also shift the key point of competition from capital to design creativity. This would play to the United States’ current strengths in design and underscores the need for more production (or acquisition) of high-end engineering talent and matching it with a supportive business environment.

Importantly and challengingly, RISC-V has already begun to be embedded across the U.S. innovation ecosystem in projects throughout the public and private sectors in applications such as [spaceflight computing](#) at NASA’s Jet Propulsion Laboratory and Nvidia’s CUDA cores. A major advantage of RISC-V is that it is a low-cost standard that can be leveraged by researchers, taught and used in universities, and adopted by small startups as well as large companies. It represents a more easily accessible, low-cost path to new innovative products and greater competition. Importantly, RISC-V is a means to bring the innovative ideas of a new generation of researchers to the market.

How the United States Can Progress Toward Standards Leadership

Historically, U.S. leadership in global standards-setting has promoted growth and innovation across technologies and their supply chains, with attendant advantages to U.S. firms. In recent years, this attention has waned.

China now recognizes the value of active participation in standards-setting in developing its long-term competitive advantage. As highlighted in the China Standards 2035 plan, China is [prioritizing](#) investment and engagement in standards-setting bodies with an eye to gaining a competitive advantage for Chinese companies in a broad range of emerging technologies. It would not be prudent to cede standards leadership. In this context, the United States should move toward exerting active leadership in international standards-setting opportunities—including that posed by RISC-V. This will require both

policy attention and greater resources for U.S. participation in standards bodies. The United States must recognize that China has changed the nature of the competition in standards, and the United States needs to adopt a constructive, but affirmative, response together with likeminded countries.

To progress toward standards leadership, the United States can leverage existing programs and mechanisms in the semiconductor innovation ecosystem. To support a pipeline of professionals fluent in RISC-V, the United States can further embed RISC-V training into engineering curricula and workforce development, such as the **Research Scholars program** funded through the Semiconductor Research Corporation. RISC-V can also be emphasized in federally funded regional initiatives like the Department of Defense **Microelectronics Commons** and Department of Commerce **Tech Hubs**, in cooperation with universities, startups, and industry. Specifically, government-supported projects provide an opportunity to support the physical infrastructure necessary to accelerate RISC-V development and validation across the ecosystem.

The U.S. government needs to ensure that the National Institute of Standards and Technology (NIST) can take an active role in the international standards process, including support for U.S. firms in standards-setting bodies such as RISC-V International. NIST can also **promote** standards education through workshops for government agencies and by convening industry leaders to better understand their interests and challenges. Stakeholders need to be provided the resources to collaborate internationally and develop strategies for standards that would best serve the interests of the United States and like-minded countries. NIST's efforts need to be adequately funded and supported to ensure that U.S. firms, viewpoints, and citizens are represented in this ongoing, international standards-setting effort.

Conclusion

To meet this challenge, the United States should promote standards education and encourage research and development in this area, including in engineering curricula, and adequately fund U.S. participation.

- **Encourage active engagement in standards-setting** by U.S. firms in international standards bodies and support NIST with the federal resources necessary to balance China's engagement.
- **Adopt programs to support RISC-V-based work** in universities and industry, especially for students to be introduced to and trained in RISC-V. **Invest in the physical infrastructure necessary to support RISC-V development**, including R&D labs and testing facilities for validating RISC-V-based hardware.
- **Use existing mechanisms**, such as proven programs from the Semiconductor Research Corporation, to support a pipeline of RISC-V-fluent professionals and programs, including RISC-V electronic design automation tools. Talent development will be key.
- **Emphasize RISC-V use and development** in federally funded projects, such as the Department of Defense Microelectronics Commons and other Tech Hubs, as a means of connecting researchers from industry and academia with tools and training to grow RISC-V leadership.

RISC-V presents a key strategic opportunity for the United States to exercise leadership and influence in the global chip design landscape in the decades to come, but the measures needed are immediate. The standards process is a moving train, and the United States needs to build a coalition to help guide

it by continuing to support the domestic design industry as a whole and support both investment and participation in RISC-V development. ■

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