CSIS TRANSLATION

Updated Japanese Export Controls on High-Performance Semiconductor Manufacturing Equipment (One Document)

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The following is a translation of a recent Japanese government document currently open for public comment related to export controls, national security, and technology policy.

The document is an English translation of parts of a proposed Japanese export control update that is relevant to advanced semiconductor manufacturing equipment. This update includes tighter restrictions on chip testing and measurement equipment, computer-aided design software, materials, and chips themselves.

The proposed update generally introduces greater specificity in which exports are covered and goes into greater technical detail than the previous controls.

Source: METI, Trade and Economic Cooperation Bureau

English Title: Request for Public Comments on Proposed Amendments to the Foreign Exchange Order and Export Trade Control Order (Important and Emerging Items, etc.)

Japanese Title: 外国為替令及び輸出貿易管理令の一部を改正する政令案等（重要・新興品目等）に対する意見募集について

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Post-amendment

Article 6

Goods with specifications defined by METI Ordinance in row 7 of Appended Table 1 of the Export Trade Control Order shall be those that correspond to any of the following:

(1) Integrated circuits (including monolithic integrated circuits, hybrid integrated circuits, multi-chip integrated circuits, film-type integrated circuits (including silicon-on-sapphire integrated circuits), optical integrated circuits, three-dimensional integrated circuits, and monolithic microwave integrated circuits) that fall under any of the following:

(a) (no update)

(b) Microprocessors, microcomputers, microcontrollers, memory devices using compound semiconductors, devices for analog-to-digital conversion, devices having analog-to-digital conversion functionality and can record or process digitized data, devices for digital-to-analog conversion, electro-optical integrated circuits, or optical integrated circuits for signal processing, field-programmable logic devices, custom integrated circuits (excluding those that can be used to determine whether the goods fall under (c) through (h), or (k) through (o), or are designed for use in goods corresponding to any of the items from rows 5 through 15 in the middle column of the Appended Table 1 of the Export Control Order; the same applies hereinafter in this article), FFT processors, static RAM or non-volatile memory that falls under one of the following (excluding integrated circuits designed for civilian automobile or railway vehicle use):

(i) to (iii) (no update);

(c) to (g) (no update);

(h) Goods employing neural networks (excluding goods falling under (o));

Pre-amendment

Article 6

Goods with specifications defined by METI Ordinance in row 7 of Appended Table 1 of the Export Trade Control Order shall be those that correspond to any of the following.

(1) Integrated circuits (including monolithic integrated circuits, hybrid integrated circuits, multi-chip integrated circuits, film-type integrated circuits (including silicon-on-sapphire integrated circuits) , optical integrated circuits, three-dimensional integrated circuits, and monolithic microwave integrated circuits) that fall under any of the following:

(a) (no update);

(b) Microprocessors, microcomputers, microcontrollers, memory devices using compound semiconductors, devices for analog-to-digital conversion, devices having analog-to-digital conversion functionality and can record or process digitized data, devices for digital-to-analog conversion, electro-optical integrated circuits, or optical integrated circuits for signal processing, field-programmable logic devices, custom integrated circuits (excluding those that can be used to determine whether the goods fall under (c) through (h), or (k) through (n), or are designed for use in goods corresponding to any of the items from rows 5 through 15 in the middle column of the Appended Table 1 of the Export Control Order; the same applies hereinafter in this article), FFT processors, static RAM or non-volatile memory that falls under one of the following (excluding integrated circuits designed for civilian automobile or railway vehicle use):

(i) to (iii) (no update);

(c) to (g) (no update);

(h) Goods employing neural networks;

(i) through (k) (no update);

(u) Integrated circuits whose total bidirectional transfer rate across all inputs and outputs with other integrated circuits not including volatile memory is 600 gigabytes per second or higher, and that correspond to one of the following, or can be programmed to correspond to any of the following:

(i) Devices having one or more digital processor units capable of executing machine language instructions with a total processing performance (TPP) of 6,000 or higher;

(ii) Devices having one or more digital basic arithmetic units with a total processing performance (TPP) of 6,000 or higher, excluding units contributing to the execution of machine language instructions specified in (i);

(iii) Devices having one or more analog basic arithmetic units with a total processing performance (TPP) of 6,000 or higher;

(iv) Devices having a combination of digital processor units and basic arithmetic units, as specified in (i) through (iii), with a total processing performance (TPP) sum of 6,000 or higher.

(2) Parts for microwave or millimeter-wave equipment that fall under any of the following:

(a) through (h) (no update);

(i) Harmonic mixers that fall under any of the following:

(i) Devices designed to extend the frequency range of a spectrum analyzer beyond 110 gigahertz;

(ii) Devices designed to extend the operating range of a signal generator, and that fall under any of the following:

1. Devices with a frequency range exceeding 110 gigahertz;

(i) through (k) (no update);

(New text)

(2) Parts for microwave or millimeter-wave equipment that fall under any of the following:

(a) through (h) (no update);

(i) Harmonic mixers that fall under any of the following:

(i) Devices designed to extend the frequency range of a spectrum analyzer beyond 90 gigahertz;

(ii) Devices designed to extend the operating range of a signal generator, and that fall under any of the following:

1. Devices with a frequency range exceeding 90 gigahertz;

2. Devices with a frequency range between 43.5 gigahertz and 110 gigahertz, and with an output exceeding 100 milliwatts (20 dBm).

(iii) Devices designed to expand the operating range of a network analyzer, and that fall under any of the following:

1. (no update);
2. Devices with a frequency range exceeding 43.5 gigahertz and not exceeding 110 gigahertz, and with an output exceeding 100 milliwatts (20 dBm).

(removed)

(iv) (no update);

(j) through (n) (no update);

(o) A parametric signal amplifier that falls under (i) through (iii) below:

(i) Those designed to operate at temperatures below -272.15 degrees Celsius;

(ii) Those designed to operate within a frequency range between 2 gigahertz and 15 gigahertz;

(iii) Those designed to operate within a frequency range between 2 gigahertz and 15 gigahertz, and with a noise figure of less than 0.015 decibels at a temperature of -272.15 degrees Celsius.

(3) through (11) (no update).

(12) Spectrum analyzers falling under any of the following:

(a) (no update);

(b) Those that operate within a frequency range between 43.5 gigahertz and 110 gigahertz, with a displayed average noise

2. Devices with a frequency range between 43.5 gigahertz and 90 gigahertz, and with an output exceeding 100 milliwatts (20 dBm).

(iii) Devices designed to expand the operating range of a network analyzer, and that fall under any of the following:

1. (no update);
2. Devices with a frequency range exceeding 43.5 gigahertz and not exceeding 31.62 gigahertz, and with an output exceeding 100 milliwatts (15 dBm);
3. Those with a frequency range exceeding 90 gigahertz but not exceeding 110 gigahertz, and with an output exceeding 1 milliwatt (0 dBm).

(iv) (no update);

(j) through (n) (no update);

(New)

(3) through (11) (no update).

(12) Spectrum analyzers falling under any of the following:

(a) (no update);

(b) Those that operate within a frequency range between 43.5 gigahertz and 90 gigahertz, with a displayed average noise

level of less than -160 dBm per hertz;

(c) Those capable of analyzing frequencies exceeding 110 gigahertz;

(d) Those falling under (i) and (ii) below:

(i) Devices with a real-time bandwidth exceeding 520 megahertz;

(ii) Those that fall under either of the following:

1. Those that detect signals with a duration of 8 microseconds or less, with attenuation from full amplitude due to gap or window effects of less than 3 decibels, and with a 100% probability of detection;

2. Those equipped with a frequency mask trigger function and capable of capturing signals with a duration of 8 microseconds or less with a 100% probability.

(13) Signal generators that fall under any of the following (excluding devices in which the output frequency is determined by adding, subtracting, or multiplying the values of the frequencies of two or more crystal oscillators):

(a) (no update);

(b) Those that operate within a frequency range between 43.5 gigahertz and 110 gigahertz, with an output exceeding 100 milliwatts (20 dBm);

(c) those that fall under any of the following:

(i) through (v) (no update);

(vi) Those that operate within a frequency range between 75 gigahertz and 110 gigahertz, with a frequency switching time of less than 100 microseconds for any frequency exceeding 5.0 gigahertz.

(d) Devices for which the ratio of the single-sideband phase noise per hertz to the carrier frequency meets any of the following conditions:

level of less than -160 dBm per hertz;

(c) Those capable of analyzing frequencies exceeding 90 gigahertz;

(d) Those falling under (i) and (ii) below:

(i) Devices with a real-time bandwidth exceeding 170 megahertz;

(ii) Those that fall under either of the following:

1. Those that detect signals with a duration of 15 microseconds or less, with attenuation from full amplitude due to gap or window effects of less than 3 decibels, and with a 100% probability of detection;

2. Those equipped with a frequency mask trigger function and capable of capturing signals with a duration of 15 microseconds or less with a 100% probability.

(13) Signal generators that fall under any of the following (excluding devices in which the output frequency is determined by adding, subtracting, or multiplying the values of the frequencies of two or more crystal oscillators):

(a) (no update);

(b) Those that operate within a frequency range between 43.5 gigahertz and 90 gigahertz, with an output exceeding 100 milliwatts (20 dBm);

(c) Those that fall under any of the following:

(i) through (v) (no update);

(vi) Those that operate within a frequency range between 75 gigahertz and 90 gigahertz, with a frequency switching time of less than 100 microseconds for any frequency exceeding 5.0 gigahertz.

(d) Devices for which the ratio of the single-sideband phase noise per hertz to the carrier frequency meets any of the following conditions:

(i) Those within a frequency range exceeding 3.2 gigahertz and not exceeding 110 gigahertz, where the frequency separation between the operating frequency and the offset frequency is between 10 hertz and 10 kilohertz, and with a value less than that calculated by the following formula:

$$20 \log_{10}\left(\text{Operating frequency expressed in megahertz.}\right) - 20 \log_{10}\left(\text{The frequency separation between the operating frequency and the offset frequency expressed in hertz.}\right) - 126$$

(ii) Those within an output frequency range between 3.2 gigahertz and 110 gigahertz, where the frequency separation between the operating frequency and the offset frequency is in a frequency range between 10 kilohertz and 100 kilohertz, and with a value less than that calculated by the following formula:

$$20 \log_{10}\left(\text{Operating frequency expressed in megahertz.}\right) - 206$$

(e) Those having a function to perform vector modulation of digital baseband signals for which the vector modulation bandwidth

(i) Those within a frequency range exceeding 3.2 gigahertz and not exceeding 90 gigahertz, where the frequency separation between the operating frequency and the offset frequency is between 10 hertz and 10 kilohertz, and with a value less than that calculated by the following formula:

$$20 \log_{10}\left(\text{Operating frequency expressed in megahertz.}\right) - 20 \log_{10}\left(\text{The frequency separation between the operating frequency and the offset frequency expressed in hertz.}\right) - 126$$

(ii) Those within an output frequency range between 3.2 gigahertz and 90 gigahertz, where the frequency separation between the operating frequency and the offset frequency is in a frequency range between 10 kilohertz and 100 kilohertz, and with a value less than that calculated by the following formula:

$$20 \log_{10}\left(\text{Operating frequency expressed in megahertz.}\right) - 206$$

(e) Those having a function to perform vector modulation of digital baseband signals for which the vector modulation bandwidth

falls under any of the following:

(i) to (iii) (no update);

(iv) Those within an output frequency range between 75 gigahertz and 110 gigahertz, and a frequency exceeding 5.0 gigahertz.

(f) Those with a maximum output frequency exceeding 110 gigahertz.

(14) Network analyzers falling under any of the following:

(a) Those that operate within a frequency range between 43.5 gigahertz and 110 gigahertz, with an output exceeding 100 milliwatts (20 dBm);

(b) deleted;

(c) Those with nonlinear vector measurement functionality within a frequency range between 50 gigahertz and 100 gigahertz [excluding those that meet the conditions in (a)];

(d) (no update).

(15) through (16-2) (no update)

(16-3) Cooling devices for ultra-low temperatures or parts thereof, which fall under any of the following:

(a) Those rated to supply a cooling output of 600 microwatts or more for over 48 hours at a temperature of -273.05 degrees Celsius or lower;

(b) A two-stage pulse tube refrigerator designed to maintain a temperature below -269.15°C, and rated to supply a cooling output of 1.5 watts or more at a temperature of -268.95°C or lower.

(17) Devices for manufacturing semiconductor elements, integrated circuits, or semiconductor materials (referred to as "semiconductor manufacturing devices" in (e) and (q)), or testing equipment, or parts or

falls under any of the following:

(i) to (iii) (no update);

(iv) Those within an output frequency range between 75 gigahertz and 90 gigahertz, and a frequency exceeding 5.0 gigahertz.

(f) Those with a maximum output frequency exceeding 90 gigahertz.

(14) Network analyzers falling under any of the following:

(a) Those that operate within a frequency range between 43.5 gigahertz and 90 gigahertz, with an output exceeding 31.62 milliwatts (20 dBm);

(b) Those that operate within a frequency range between 90 gigahertz and 110 gigahertz, with an output exceeding 1 milliwatts (0 dBm);

(c) Those with nonlinear vector measurement functionality within a frequency range between 50 gigahertz and 100 gigahertz [excluding those that meet the conditions in (a) or (b)];

(d) (no update).

(15) through (16-2) (no update)

(New text)

(17) Those devices or test devices for manufacturing semiconductor elements, integrated circuits, or semiconductor materials (referred to as "semiconductor manufacturing devices" in (e) and (f)), or masks or reticles for

accessories thereof.

(a) Crystal epitaxial growth devices that fall under any of the following (excluding those that fall under (x)):

(i) (no update);

(ii) Organometallic chemical vapor deposition reactors designed for epitaxial growth of compound semiconductors containing at least two elements selected from aluminum, gallium, indium, arsenic, phosphorus, antimony, oxygen, or nitrogen;

(iii) (no update);

(b) through (e) (no update);

(f) Lithography devices that fall under any of the following:

(i) (no update);

(ii) Imprint lithography devices capable of achieving a line width of 45 nanometers or less (excluding those corresponding to (ai));

(iii) and (iv) (no update);

(g) deleted;

(h) deleted;

(i) deleted;

(j) through (m) (no update);

(n) Devices designed for dry etching that fall

manufacturing testing equipment or integrated circuits that fall under any of the following, or parts or accessories thereof (excluding those falling under the following paragraph).

(a) Crystal epitaxial growth devices that fall under any of the following (excluding those that fall under (x)):

(i) (no update);

(ii) Organometallic chemical vapor deposition reactors designed for epitaxial growth of compound semiconductors containing at least two elements selected from aluminum, gallium, indium, arsenic, phosphorus, antimony, or nitrogen;

(iii) (no update);

(b) through (e);

(f) Lithography devices that fall under any of the following:

(i) (no update);

(ii) Imprint lithography devices capable of achieving a line width of 45 nanometers or less;

(iii) and (iv) (no update);

(g) Masks or reticles for the manufacture of integrated circuits that fall under any of paragraphs 1 to 8-4;

(h) Multilayer masks with a phase shift film, designed for use in a lithography apparatus with a light source wavelength of less than 245 nanometers (excluding those that fall under (g), and those designed for the manufacture of memory devices that do not fall under any of paragraphs 1 to 8-4;

(i) Imprint lithography templates for the manufacture of integrated circuits that fall under any of paragraphs 1 to 8-4;

(j) through (m) (no update);

(n) Devices designed for dry etching that fall

under any of the following:

(i) (no update);

(ii) Devices designed or modified for anisotropic dry etching, and which meet all of the following conditions (excluding those corresponding to (aj) (i) or (ak)):

1. (no update);
2. Devices having one or more high-speed gas switching valves with a switching time of less than 50 milliseconds;
3. Electrostatic chucks (limited to those having 10 or more individually temperature-controllable areas).

(o) (no update);

(p) Devices designed for anisotropic etching, capable of forming a dielectric material with a shape in which the ratio of the depth to the width of the etching exceeds 30 times and the dimension of the width is less than 100 nanometers, and that fall under all of the following (excluding those that apply to [(n) (ii), (o), (aj) (i), or (ak)]:

(i) Those with one or more power sources for high-frequency pulse output;

(ii) Those having one or more high-speed gas switching valves with a switching time of less than 300 milliseconds.

(q) Semiconductor manufacturing devices, which are film deposition devices and fall under any of the following:

(i) and (ii) (no update);

(iii) Devices designed to deposit a metal contact layer through multiple processes within a single chamber, and that fall under all of the following [excluding those apply to ii)]:

1. (no update);
2. Those having plasma surface

under any of the following:

(i) (no update);

(ii) Devices designed or modified for anisotropic dry etching that fall under all of the following:

1. (no update);
2. Those having one or more high-speed gas switching valves with a switching time of less than 300 milliseconds;
3. Those with electrostatic chucks (limited to those having 20 or more individually temperature-controllable areas).

(o) (no update);

(p) Devices designed for anisotropic etching, which are capable of forming a dielectric material with a shape in which the ratio of the depth to the width of the etching exceeds 30 times and the width is less than 100 nanometers, and which fall under all of the following [excluding those falling under (n) or (o)]:

(i) Those with one or more power sources for high-frequency pulse output;

(ii) Those having one or more high-speed gas switching valves with a switching time of less than 300 milliseconds.

(q) Semiconductor manufacturing devices, which are film deposition devices and fall under any of the following:

(i) and (ii) (no update);

(iii) Devices designed to deposit a metal contact layer through multiple processes within a single chamber, and that fall under all of the following [excluding those apply to ii)]:

1. (no update);
2. Those having plasma processes

treatment processes that use hydrogen, a mixture of hydrogen and nitrogen, or ammonia).

(iv) Semiconductor manufacturing devices designed to deposit films through multiple processes within multiple chambers or stations (hereinafter referred to as "specified semiconductor manufacturing equipment"); and designed to deposit metal contact layers through all of the processes set forth as follows (excluding those that apply to (ii)):

1. to 3. (no update);

(v) through (x) (no update);

(r) Among specific semiconductor manufacturing equipment, devices designed to deposit a layer of metal and which meet all of the following conditions (excluding those that fall under (q)(ii)):

(i) and (ii) (no update);

(s) Among specific semiconductor manufacturing equipment, devices designed to deposit a layer of metal and which meet all of the following conditions [excluding those that fall under (q)(ii)]:

(i) and (ii) (no update);

(t) and (u) (no update).

(v) Film deposition devices that fall under any of the following (excluding those that fall under (al) (iii)):

(i) and (ii) (no update);

(w) (no update);

(x) Devices designed for the epitaxial growth of silicon or silicon germanium that fall under all of the following:

that use hydrogen (including mixtures of hydrogen with nitrogen or ammonia).

(iv) Semiconductor manufacturing devices designed to deposit films through multiple processes within multiple chambers or stations and to maintain a vacuum or inert environment of 0.01 pascal or less between the multiple processes (hereinafter referred to as "specified semiconductor manufacturing equipment"), and designed to deposit metal contact layers through all of the processes set forth as follows (excluding those that apply to (d)):

1. to 3. (no update);

(v) through (x) (no update);

(r) Devices designed to deposit a layer of metal in a vacuum or inert gas environment of less than 0.01 pascal, and which meet all of the following conditions [excluding those falling under (q) (ii)]:

(i) and (ii) (no update);

(s) Devices designed to deposit a layer of metal in a vacuum or inert gas environment of less than 0.01 pascal, and which meet all of the following conditions [excluding those falling under (q) (ii)]:

(i) and (ii) (no update);

(t) and (u) (no update)

(v) Film deposition devices that fall under any of the following:

(i) and (ii) (no update);

(w) (no update);

(x) Devices designed for the epitaxial growth of silicon (including that which contains added carbon) or silicon germanium (including that which contains added carbon) that fall under all of the following:

(remove)

(i) and (ii) (no update).

(y) Devices designed to deposit carbon hard masks, with a thickness exceeding 2 micrometers and a density exceeding 1.7 grams per cubic centimeter, using a plasma-assisted chemical vapor deposition method.

(z) (no update).

(aa) Devices designed to deposit, using plasma, low dielectric layers with a relative permittivity of less than 3.3 between metal wiring (where the width is less than 25 nanometers and the depth-to-width ratio is at least 1), thereby preventing void formation (excluding those falling under (al) (iii)).

(ab) through (af) (no update).

(ag) Ion implantation equipment designed for plasma doping, and which falls under all of the following:

(i) Those with one or more power sources for high-frequency pulse output;

(ii) Those with one or more power sources of DC pulse power;

(iii) Those capable of injecting at least one N-type or P-type impurity.

(ah) Devices designed or modified to perform any of the following, in a deep ultraviolet liquid immersion photolithography apparatus, or in conjunction with a deep ultraviolet liquid immersion photolithography apparatus:

(i) Those that fall under all of the following:

(i) Those having multiple chambers and being capable of maintaining a vacuum of less than 0.01 pascal or an inert environment with a partial pressure of water and oxygen of less than 0.01 Pascals between the multiple processes;

(i) and (ii) (no update).

(y) Devices designed to deposit carbon hard masks, with a thickness exceeding 100 nanometers and with a stress of less than 450 megapascals, using a plasma-assisted chemical vapor deposition method;

(z) (no update).

(aa) Devices designed to deposit, using plasma, low dielectric layers with a relative permittivity of less than 3.3 in the gaps between metal wiring (where the width is less than 25 nanometers and the depth-to-width ratio is equal or greater than 1), thereby preventing void formation;

(ab) through (af) (no update).

(New text)

1. Deep ultraviolet liquid immersion photolithography devices designed to reduce the value obtained by multiplying the wavelength of the light source (expressed in nanometers) by 0.25 and dividing the result by the numerical aperture, so that the final value is 45 or less;

2. Deep ultraviolet liquid immersion photolithography devices designed to achieve an overlay accuracy of 2.4 nanometers or less:

(ii) Exposure devices that fall under (f)(1) or (o), designed or modified to increase the average number of wafers processed per hour by at least one percent during a given time interval.

(ai) Imprint lithography devices capable of achieving an overlay accuracy of 4.0 nanometers or less.

(aj) Devices designed for etching that fall under any of the following:

(i) Those devices designed for anisotropic dry etching that fall under all of the following:

1. Those having two or more independent high-frequency power supplies;

2. Those having two or more independent gas supply sources;

3. Those having a process uniformity adjustment function to correct uneven wafer thickness;

4. Those having a function to detect the endpoint of the silicon through electrode exposure process.

(ii) Devices designed for anisotropic etching, capable of forming a dielectric material with a high depth-to-width ratio, and which fall under all of the following (excluding those that fall

(New Text)

(New Text)

under (n) (ii), (o), (p), (aj) (i), or (ak)):

1. Those with an etching depth-to-width ratio exceeding 30;
2. Those having a top etching width less than 40 nanometers.

(New Text)

(iii) Devices designed for etching to create silicon through-electrodes, and which fall under all of the following (excluding those that fall under (n), (o), (p), (aj)(i), or (aj)(ii)):

1. Those in which the silicon etching speed exceeds 7 micrometers per minute;
2. Those in which the etching depth non-uniformity within the wafer is 2% or less;
3. Those in which the aspect ratio of the silicon through-electrode is 10 or more.

(ak) Devices Designed for extreme ultraviolet pattern shaping (excluding those falling under (n)(i), (o), or (aj)(i).

(al) Semiconductor manufacturing devices, which are film deposition devices and fall under any of the following:

(i) Those that deposit a tungsten film using physical vapor deposition, are equipped with an electromagnet for inducing ion flux, and are specifically designed to deposit on shapes with an aspect ratio of 3 or higher;

(ii) Those designed or modified to deposit a film of molybdenum, ruthenium, or a combination of both using atomic layer deposition, and which fall under all the following (excluding those falling under (t)):

1. Those designed or modified to operate at a temperature exceeding 75 degrees Celsius, which have a metal precursor supply source;

(New Text)

2. Those having a process chamber using a reducing agent containing hydrogen at a pressure of 4 kilopascals or higher.

(iii) Those designed to perform film deposition through chemical vapor deposition using plasma or radicals, which, while maintaining the substrate temperature below 500 degrees Celsius, cures a dielectric film with ultraviolet light on a single device, and can deposit a dielectric film that meets all of the following criteria:

1. Those having a metal shape with a thickness exceeding 6 nanometers but less than 20 nanometers, a pitch of less than 24 nanometers, and an aspect ratio of 1.8 or more;

2. Those having a relative permittivity of less than 5.3.

(iv) Those designed to perform film deposition of carbon materials using chemical vapor deposition, using materials with a density exceeding 1.6 grams per cubic centimeter (excluding those falling under (y)).

(v) Film deposition devices that directly inject two or more types of metal precursors into a single deposition chamber, and are designed or modified to form an isotropic dielectric film with a relative permittivity exceeding 35, in a shape with a depth-to-width ratio exceeding 50 times.

(am) Annealing devices designed for 300 millimeter wafers, which can heat the wafers to a temperature exceeding 1,000 degrees Celsius for a duration of less than 2 milliseconds.

(an) Single-wafer cleaning devices designed to use supercritical carbon dioxide or sublimination drying.

(ao) Patterned wafer defect measurement

(New Text)

(New Text)

devices or patterned wafer defect inspection devices, designed or modified to accommodate wafers with a diameter of 300 millimeters or more, and which fall under all of the following:

(New Text)

(i) Those designed or modified to detect defects of 21 nanometers or smaller;

(ii) Those falling under any of the following:

1. A light source with a wavelength of less than 400 nanometers;
2. An electron beam source with a resolution of 1.65 nanometers or less;
3. A beam cold-cathode field emission electron beam source;
4. Two or more electron beam sources.

(ap) Measuring devices that fall under any of the following:

(i) Stand-alone devices designed to use the measured values of the wafer shape parameters, measured before exposure, to improve the overlay error or focus of a deep ultraviolet lithography system or extreme ultraviolet lithography system with an immersion lens having a numerical aperture greater than 1.3;

(ii) Measurement devices designed to measure focus or overlay error on a product wafer, after resist development or etching, using image-based overlay error or diffraction-based measurement techniques, and having an overlay error measurement accuracy of 0.5 nanometers or less, and falling under one of the following:

1. Those designed to be integrated into a track;
2. Those having a high-speed wavelength switching function.

(New Text)

(17-2) Devices or testing equipment for the manufacture of semiconductor elements, integrated circuits, or semiconductor materials, which fall under any of the following:

(a) Scanning electron microscopes designed to obtain images of semiconductor elements or integrated circuits, and which meets all of the criteria from (i) to (vii) below (excluding those designed for wafer loading parts for wafer transport and storage containers (including 200mm or larger Front Opening Unified Pods (FOUP)), in compliance with the SEMI standards set by the Semiconductor Equipment and Materials Institute):

(i) Those with stages that possess a positioning accuracy of less than 30 nanometers;

(ii) Those capable of measuring stage position using a laser interferometer;

(iii) Those capable of field-of-view calibration based on length scale measurement using a laser interferometer;

(iv) Those capable of collecting and storing images with pixel counts exceeding 200,000,000;

(v) Those having less than 5% overlap in the field of view in both the vertical and horizontal directions when acquiring images;

(vi) Those having less than 50 nanometers of overlap in the field of view when combining images;

(vii) Those having an acceleration voltage exceeding 21 kilovolts.

(b) Cryogenic wafer probers designed to operate at extremely low temperatures, and falling under (i) and (ii) below:

(i) Those designed to operate at temperatures below -268.65 degrees

(17-2) Pellicles designed especially for devices for manufacturing integrated circuits using extreme-ultraviolet radiation.

Celsius;

(ii) Designed to accommodate wafers with a diameter of 100 millimeters or more.

(17-3) Masks or reticles for manufacturing integrated circuits, or parts or accessories thereof, that fall under any of the following:

(a) Masks or reticles (excluding those that fall under (d)), for the manufacture of integrated circuits, or their parts or accessories, which fall under any of the provisions of items 1 through 8-4 (excluding those listed in (e));

(b) Multilayer masks with a phase shift film, designed for use in a lithography apparatus with a light source wavelength of less than 245 nanometers (excluding those that fall under (a) or (d), and those designed for the manufacture of memory devices that do not fall under any of the provisions of items 1 to 8-4, or parts or accessories thereof;

(c) Imprint lithography templates for the manufacture of integrated circuits that fall under any of the items 1 to 8-4, or its parts or accessories;

(d) Masks or reticles specially designed for use in equipment for manufacturing integrated circuits using extreme ultraviolet (EUV), which includes a mask blank that falls under the following item, or any of its parts or accessories [excluding those listed under (e)];

(e) Pellicles that are designed especially for use in devices for manufacturing integrated circuits using extreme-ultraviolet radiation.

(17-4) [no update]

(removed)

(17-3) (no update).

(New text)

(17-4) Scanning electron microscopes designed to obtain images of semiconductor elements or integrated circuits, and which meet all of the criteria from (a) to (g) below (excluding those designed for wafer loading parts for wafer transport and storage containers (including 200mm or larger Front Opening

Unified Pods (FOUP)), in compliance with the SEMI standards set by the Semiconductor Equipment and Materials Institute):

(a) Those with stages that possess a positioning accuracy of less than 30 nanometers;

(b) Those capable of measuring stage position using a laser interferometer;

(c) Those capable of field-of-view calibration based on length scale measurement using a laser interferometer;

(d) Those capable of collecting and storing images with pixel counts exceeding 200,000,000;

(e) Those having less than 5% overlap in the field of view in both the vertical and horizontal directions when acquiring images;

(f) Those having less than 50 nanometers of overlap in the field of view when combining images;

(g) Those having an acceleration voltage exceeding 21 kilovolts.

(18) Substrates having a crystalline multilayer film of a substance from the following categories on its surface, where the crystals are epitaxially grown. This applies to substrates with heteroepitaxial materials (excluding those that fall under the following item or are compounds falling under (d) (which include Gallium Nitride, Indium Gallium Nitride, Aluminum Gallium Nitride, Indium Aluminum Nitride, Indium Aluminum Gallium Nitride, Gallium Phosphide, Gallium Arsenide, Aluminum Gallium Arsenide, Indium Phosphide, Indium Gallium Phosphide, Aluminum Indium Phosphide, or Indium Gallium Aluminum Phosphide). The substrate must have at least one P-type epitaxial layer, excluding those where the P-type epitaxial layer is sandwiched between N-type layers.

(a) (no update).

(18) Substrates having a crystalline multilayer film of a substance from the following categories on its surface, where the crystals are epitaxially grown. This applies to substrates with heteroepitaxial materials, (limited to compounds falling under (d), which include Gallium Nitride, Indium Gallium Nitride, Aluminum Gallium Nitride, Indium Aluminum Nitride, Indium Aluminum Gallium Nitride, Gallium Phosphide, Gallium Arsenide, Aluminum Gallium Arsenide, Indium Phosphide, Indium Gallium Phosphide, Aluminum Indium Phosphide, or Indium Gallium Aluminum Phosphide). The substrate must have at least one P-type epitaxial layer, excluding those where the P-type epitaxial layer is sandwiched between N-type layers.

(a) (no update).

(18-2) Substrates having a crystalline film, consisting of one or more layers of a substance from the following categories, epitaxially grown on its surface, and suitable for epitaxial material use.

(a) Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30.

(b) Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

(19) through (24) (no update).

(25) Silicon or germanium fluorides, hydrides, or chlorides, containing any of the following:

(a) Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30.

(b) Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

(26) Silicon, silicon oxide, germanium, or germanium oxide, including any of the following, or these substrates or ingots, boule, or other preforms.

(a) Silicon having an isotopic impurity less than 0.08% of silicon isotopes other than silicon-28 or silicon-30.

(b) Germanium having an isotopic impurity less than 0.08% of germanium isotopes other than germanium-70, germanium-72, germanium-74, or germanium-76.

Article 7

Those with specifications defined by METI Ordinance in row 8 of Appended Table 1 of the Export Trade Control Order shall be those that fall under any of the following:

(1) through (6) (no update).

(7) Electronic computers or their electronic assemblies or components, including

(New text)

(19) through (24) (no update).

(New text)

Article 7

Those with specifications defined by METI Ordinance in row 8 of Appended Table 1 of the Export Trade Control Order shall be those that fall under any of the following:

(1) through (6) (no update).

(New text)

integrated circuits that fall under paragraph 1 (o) of the previous article.

(7) through (20) (no update).

Article 17

Technologies specified by METI Ordinance in row 1, item 5 of the Appended Table of the Foreign Exchange Order shall be those that fall under any of the following:

2. to 6. (no update);

7. Technologies specified by METI Ordinance in row 5, item 8 of the Appended Table of the Foreign Exchange Order shall be the technology (excluding programs) pertaining to the use of radio waves or infrared absorbers or conductive polymers, as specified in Article 14, paragraph 2 (limited to those related to installation, maintenance, or repair.)

Article 18

(no update)

2. to 5. (no update);

6. Technologies specified by METI Ordinance in row 6, team 6 of the Appended Table 6 the Foreign Exchange Order shall pertain to technologies related to the design or manufacturing of coating systems as specified in the following items (excluding programs):

   (1) Those designed to prevent corrosion of ceramic matrix composites that fall under Article 4, paragraph 12;

   (2) Those designed to be used at temperatures exceeding 1,100 degrees.

Article 19

Technologies specified by METI Ordinance in row 7, item 1of the Appended Table of the Foreign Exchange Order shall be those that fall under any of the following:

(1) through (4) (no update);

(5) Programs designed for the purpose of designing or manufacturing those that fall under Article 6 (excluding those that fall under either of the previous

(7) through (20) (no update).

Article 17

Technologies specified by METI Ordinance in row 1, item 5 of the Appended Table of the Foreign Exchange Order shall be those that fall under any of the following:

2. to 6. (no update);

7. Technologies specified by METI Ordinance in row 5, item 8 of the Appended Table of the Foreign Exchange Order shall be the technology (excluding programs) pertaining to the use of radio waves absorbers, or conductive polymers, as specified in Article 14, paragraph 2 (limited to those related to installation, maintenance, or repair).

Article 18

(no update).

2. to 5. (no update);

(New text)

Article 19

Technologies specified by METI Ordinance in row 7, item 1of the Appended Table of the Foreign Exchange Order shall be those that fall under any of the following:

(1) through (4) (no update);

(5) Programs designed for the purpose of designing or manufacturing those that fall under Article 6 (excluding those that fall under either of the previous two

two paragraphs, or under paragraph 1, paragraph 16-3, or paragraphs 18 through 26 of Article 6.)

2. Technologies specified by METI Ordinance in row 7, item 2 of the Appended Table of the Foreign Exchange Order shall pertain to programs designed to use those that fall under Article 6, paragraph 17, subparagraphs (a), (b), (h), (e), or (f) through (ap).

3. Technologies specified by METI Ordinance in row 7, item 3 of the Appended Table of the Foreign Exchange Order shall be those that fall under any of the following:

(1) through (8) (no update);

(9) Electronic computer-aided design programs designed to integrate multiple chips into multi-chip integrated circuits, and which meet all of the following conditions:

(i) Those with floor planning;

(ii) Those with chip and package co-design or co-simulation.

(10) Electronic computer-aided design programs designed or modified for the design or manufacture of integrated circuits using multi-patterning.

(11) Computer lithography programs designed or modified to design or manufacture patterns on masks or reticles for deep ultraviolet lithography.

4. and 5. (no update).

Article 20

Technologies specified by METI Ordinance in row, item 1 of the Appended Table of the Foreign Exchange Order shall fall under one of the following (technologies related to the disclosure of security vulnerabilities or response to cyberattacks (excluding programs)):

(1) Technologies (excluding programs) necessary for the design, manufacture, or use of those that fall under Article 7,

paragraphs, or under paragraph 1 or paragraphs 16 through 24 of Article 6.)

2. Technologies specified by METI Ordinance in row 7, item 2 of the Appended Table of the Foreign Exchange Order shall pertain to programs designed to use those that fall under Article 6, paragraph 17, subparagraphs (a), (b), (h), (e), or (f) through (af).

3. Technologies specified by METI Ordinance in row 7, item 3 of the Appended Table of the Foreign Exchange Order shall be those that fall under any of the following:

(1) through (8) (no update);

(New text)

4. and 5. (no update).

Article 20

Technologies specified by METI Ordinance in row , item 1 of the Appended Table of the Foreign Exchange Order shall fall under one of the following [technologies related to the disclosure of security vulnerabilities or response to cyberattacks (excluding programs):

(1) Technologies (excluding programs) necessary for the design, manufacture, or use of those that fall under Article 7,

paragraph 1 to paragraph 5 or paragraph 7;

(2) Programs designed to design or manufacture those that fall under Article 7, paragraph 1 to paragraph 5 or paragraph 7, or technologies (excluding programs) necessary for the design, manufacture, or use of such programs;

(3) and (4) (no update).

2. (no update)

paragraphs 1 through 5;

(2) Programs designed for the purpose of designing or manufacturing those falling under Article 7, paragraph 1 to paragraph 5, or technologies (excluding programs) necessary for the design, manufacture, or use of such programs;

(3) and (4) (no update).

2. (no update)