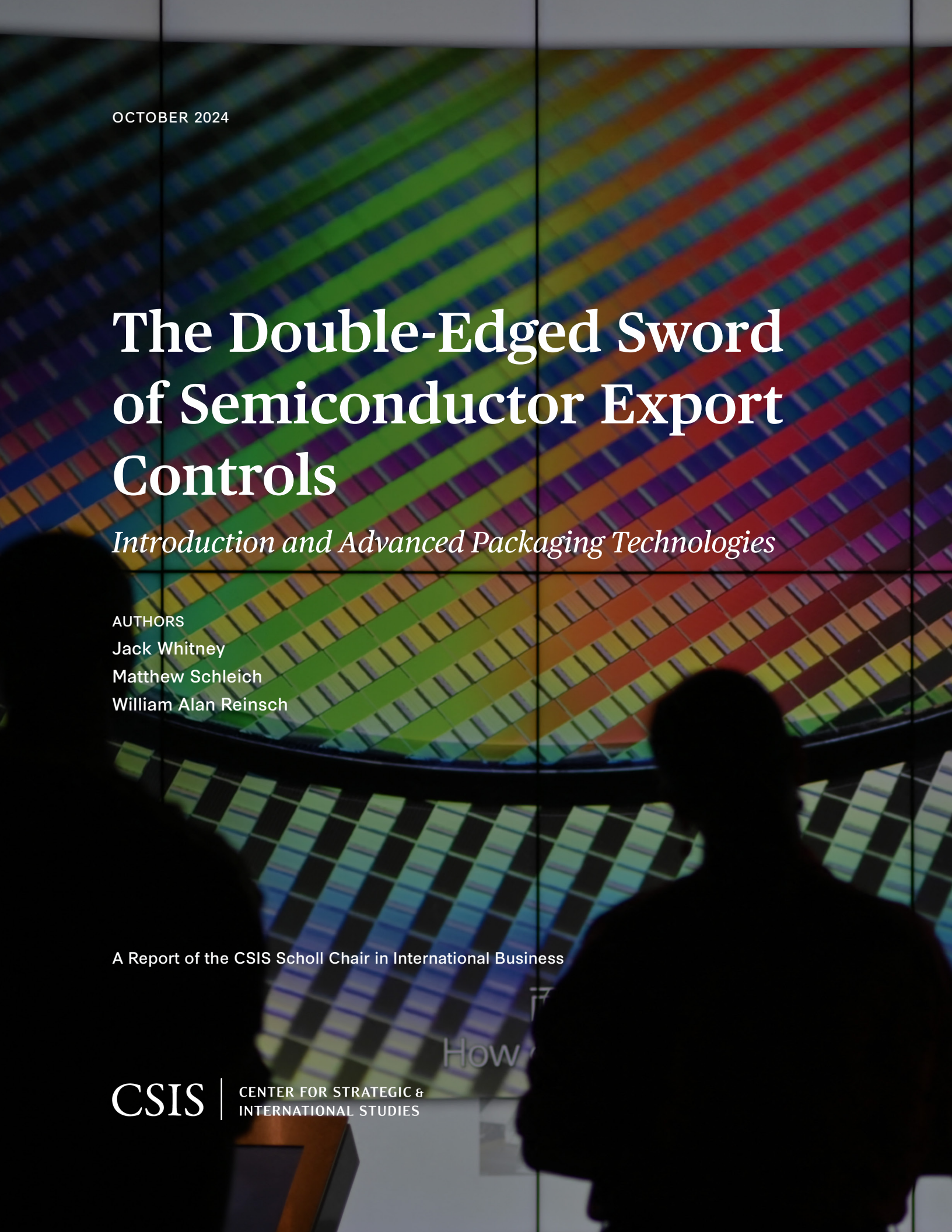


OCTOBER 2024

The Double-Edged Sword of Semiconductor Export Controls

Introduction and Advanced Packaging Technologies

AUTHORS
Jack Whitney
Matthew Schleich
William Alan Reinsch

A Report of the CSIS Scholl Chair in International Business

CSIS | CENTER FOR STRATEGIC & INTERNATIONAL STUDIES

OCTOBER 2024

The Double-Edged Sword of Semiconductor Export Controls

Introduction and Advanced Packaging Technologies

AUTHORS
Jack Whitney
Matthew Schleich
William Alan Reinsch

A Report of the CSIS Scholl Chair in International Business

CSIS | CENTER FOR STRATEGIC & INTERNATIONAL STUDIES

About CSIS

The Center for Strategic and International Studies (CSIS) is a bipartisan, nonprofit policy research organization dedicated to advancing practical ideas to address the world's greatest challenges.

Thomas J. Pritzker was named chairman of the CSIS Board of Trustees in 2015, succeeding former U.S. senator Sam Nunn (D-GA). Founded in 1962, CSIS is led by John J. Hamre, who has served as president and chief executive officer since 2000.

CSIS's purpose is to define the future of national security. We are guided by a distinct set of values—nonpartisanship, independent thought, innovative thinking, cross-disciplinary scholarship, integrity and professionalism, and talent development. CSIS's values work in concert toward the goal of making real-world impact.

CSIS scholars bring their policy expertise, judgment, and robust networks to their research, analysis, and recommendations. We organize conferences, publish, lecture, and make media appearances that aim to increase the knowledge, awareness, and salience of policy issues with relevant stakeholders and the interested public.

CSIS has impact when our research helps to inform the decisionmaking of key policymakers and the thinking of key influencers. We work toward a vision of a safer and more prosperous world.

CSIS does not take specific policy positions; accordingly, all views expressed herein should be understood to be solely those of the author(s).

Center for Strategic & International Studies
1616 Rhode Island Avenue, NW
Washington, DC 20036
202-887-0200 | www.csis.org

Acknowledgments

The CSIS Scholl Chair in International Business is grateful to the numerous experts who provided their valuable time and input to support this project over the last six months. In particular, the authors are grateful to the private sector participants who agreed to be interviewed under the Chatham House Rule for this report. We would also like to thank all the attendees of the Scholl Chair's July 25, 2024, roundtable discussion covering the design-out challenge in semiconductor supply chains.

The authors are also grateful to a handful of CSIS experts for their assistance with research and feedback. These include Barath Harithas, Senior Fellow in the Project on Trade and Technology, who offered key insights on semiconductor manufacturing and export controls, and Thibault Denamiel, Associate Fellow with the Scholl Chair in International Business, who served as a valuable thought partner and reviewer.

This report is made possible through generous support from Applied Materials and Onto Innovation.

Contents

Introduction

The United States has undertaken a significant shift in its economic security strategy in recent years. As geopolitical competition with China has accelerated, U.S. policymakers have increasingly leveraged restrictions on critical and emerging technologies (CETs) to safeguard U.S. leadership in military and dual-use applications such as artificial intelligence (AI). Export controls have reemerged as a widely utilized economic security tool in the U.S. arsenal, with the aim of slowing Chinese technological progression by limiting access to U.S. and allied nations' products. Advanced semiconductors have been a key focus of these efforts due to their national security implications, chief among them the enablement of advanced AI systems.

The Trump administration's actions toward Chinese telecommunications giant ZTE marked an early, pivotal moment in the United States' expanded use of export controls. In April 2018, President Donald Trump imposed tough restrictions on ZTE's access to a range of U.S. technologies, including semiconductors, putting the company on the verge of bankruptcy.[1] Despite Trump's later reversal, the episode showcased a renewed embrace of export controls by Washington as a tool of economic coercion.[2] Another key moment came in a 2022 speech by National Security Advisor Jake Sullivan, in which he announced that the United States must "maintain as large of a lead as possible" over China in the fields of advanced logic and memory chips.[3] This was a departure from the longstanding "sliding scale" approach, in which the United States sought to stay "a couple generations ahead" of strategic competitors like China but did not impose broad measures to restrict technological progression.[4]

Under the Biden administration, the U.S. government has implemented two major rounds of semiconductor export controls targeting advanced semiconductor supply chains in countries of concern, most notably China.[5] As of this report's release, Washington remains engaged in discussions around enacting further measures.[6] The U.S. goal is to ensure that Chinese semiconductor capabilities remain well behind the global technological frontier in the interest of protecting U.S. national security.

However, as the U.S. government has expanded efforts to control global semiconductor markets, Chinese officials and businesses have responded—often in ways not entirely anticipated by U.S. policymakers. For one, Chinese policymakers and businesses have employed various methods to circumvent U.S. export controls.[7] These include importing controlled U.S. technologies from third countries via overseas shell companies, redirecting semiconductor technologies to prohibited entities via domestic technology trading networks, misleading foreign suppliers about the end uses of imported technologies, and stockpiling equipment before regulations take effect.[8]

While circumvention efforts have been a key topic of discussion for the U.S. export controls, less attention has been paid to the other key impact of the controls: catalyzing a government- and industry-wide effort within the Chinese semiconductor industry to *do away with U.S. companies and technology entirely.*[9] While Beijing has for decades been interested in building domestic semiconductor production, the Biden administration's controls transformed the timeline and scale of these efforts.[10] China's government and commercial sector have begun undertaking a supply chain transformation aimed at reducing reliance on U.S. semiconductor technologies wherever possible.[11] These efforts aim to mitigate the impact of current export controls and reduce the long-term vulnerability of China's semiconductor ecosystem to future U.S. trade actions.

China's semiconductor ecosystem is following two main pathways to achieve this goal: design-out and design-around. Together, these strategies threaten to render U.S. export control policies—even when comprehensively enforced—less effective as a longer-term barrier to Chinese technological progression in advanced semiconductors. More importantly, they also threaten to weaken U.S. semiconductor industry leadership overall by hindering U.S. companies' market access and revenue—and consequently, their long-term leadership in research and development (R&D):

1. **Design out:** supplanting existing U.S. and allied semiconductor technologies with *comparable* technologies, from either
    a. Chinese firms; or
    b. third-country (non-U.S. and non-Chinese firms)
2. **Design around:** developing *new* technologies that do away with an entire category of controlled technology in the semiconductor supply chain

China's design-out and design-around efforts are threats to U.S. policymakers and domestic business leaders working to develop a strong domestic technological industrial base and compete with powerful dual-use technologies. Therefore, they are threats to U.S. national and economic security.

This report argues that if they are not responded to properly, design-out and design-around efforts mean that U.S. export control policy could unintentionally undermine the United States' long-term positioning in its geopolitical and economic competition against China to "win the 21st century."[12]

The Design-Out Strategy

Chinese policymakers are increasingly concerned about dependence on U.S. technology within China's semiconductor supply chain.[13] Private sector interests, namely Chinese semiconductor companies, have also come to realize the business risks of overreliance on U.S. technology. To minimize the impact of current restrictions and hedge against a future tightening of controls, Chinese policymakers and semiconductor companies are working to "design out" U.S. technology from China's semiconductor ecosystem—in other words, to replace U.S. suppliers with alternatives wherever possible.

Today, non-U.S. production lines are being built out in two ways. First, China's central and local governments are investing billions to help domestic firms produce the designs, components, and tools necessary for manufacturing semiconductors.[14] At the same time, there is new government pressure on Chinese semiconductor companies to procure key technologies domestically.[15] These manufacturers, themselves wary of the commercial risks of reliance on foreign technology, are also increasingly eager to buy from Chinese suppliers.

Second, companies from third countries (i.e., countries other than the United States and China)—whose governments are resistant to expanding export controls on China due to concerns about lost revenue and access to Chinese markets—are filling in the gaps left behind by U.S. companies.[16] As Chinese semiconductor manufacturing facilities, known as fabs, buy less and less technology from U.S. suppliers, market opportunities are opening up for firms from third countries, which are not fully aligned with the United States on control policy or enforcement.

The U.S. controls are designed to apply extraterritorially, which ostensibly complicates import substitution. However, this has not necessarily been the case in practice. Despite the U.S. foreign direct product rules (FDPRs) and de minimis restrictions associated with the controls, which limit foreign companies' use of some U.S. technology content, there is strong evidence to suggest that import substitution by foreign countries is occurring.[17] Although the Netherlands and Japan imposed new controls in 2023 that replicated aspects of U.S. restrictions, key differences remain in scope and enforcement capabilities—for instance, the ability of foreign companies to offer on-site servicing to Chinese customers.[18] Notable supply countries—such as Germany, South Korea, and Israel—have also not imposed comparable controls. The United States, for its part, continues to pressure allies to expand export regimes to achieve harmonization, but success has proven challenging.[19]

Foreign Direct Product Rules

FDPRs apply the U.S. Export Administration Regulations (EAR) to foreign-made items if they are the "direct product" of certain types of U.S.-origin equipment, software, or other technology, and are destined for designated countries. Specifically, FDPRs empower the Bureau of Industry and Security (BIS) to require licenses for exports of certain foreign-made products if listed U.S. technology was directly used to produce them or produce key parts of the plants that were used to manufacture the products, such as a tool or a piece of software—even if a controlled U.S. component or system does not appear in the product.[20]

Three FDPRs limit Chinese access to semiconductor technologies: the Entity List (EL), Advanced Computing, and Supercomputer FDPRs.[21] These FDPRs differ in terms of the products, companies, and countries that they cover. The EL FDPR, introduced in May 2020 by the Trump administration, applies U.S. export controls to products destined for hundreds of Chinese (and other foreign) companies and their subsidiaries.[22] These restrictions vary based on the products involved as well as the type of EL classification applicable to the purchaser company. Their reach has continued to grow as the U.S. Department of Commerce has added Chinese firms to the EL.[23] The Advanced Computing FDPR applies the EAR to a narrower range of products meeting certain performance parameters and based on the destination country rather than the destination company. Originally aimed at China, the Advanced Computing FDPR has expanded the list of destination countries to include the countries China likely uses to avoid controls, such as Kazakhstan and Mongolia.[24] Finally, the Supercomputer FDPR applies a country and end-use scope to encompass any items subject to the EAR that are used to produce supercomputers, which are defined based on compute capacity and system dimensions.[25]

De Minimis Rules

De minimis rules apply the EAR based on the inclusion of U.S.-origin controlled inputs in foreign-exported goods destined for specific countries. Notably, unlike the FDPRs, use of de minimis rules requires that the exported goods directly contain products produced in the United States that fall under the EAR.[26] This differs from the FDPR's broader threshold of goods being the "direct product" of certain U.S.-origin technologies or inputs (that do not need to be included in the actual goods being shipped). In cases where the shipment of the U.S. inputs to the final country destination by themselves (i.e., when not incorporated into a final product) would require a license, a de minimis calculation is necessary for the foreign export of the product that contains the inputs. Depending on the type of product and country destination, different de minimis thresholds—or the minimum percentage of U.S.-origin controlled items as a share of "fair market value" at which the EAR applies (typically 10 or 25 percent)—are relevant to the specific good.[27] If the good exceeds the

relevant de minimis threshold, an export waiver is required, pursuant to the EAR. For some products (e.g., certain lithography tools), a zero percent de minimis threshold applies, meaning that inclusion of any U.S.-origin controlled input automatically applies the EAR.[28]

The Design-Around Strategy

Beyond its efforts to replace U.S. technologies one-for-one using domestic and third-country suppliers, China also seeks to develop novel capabilities that offer alternative methods to achieve the same performance capabilities provided by leading-edge chips in microelectronics systems. These innovations would enable China's semiconductor ecosystem to achieve the capabilities required for applications such as advanced AI, and to do so using technologies that originate in Chinese—rather than U.S. or partner nations'—intellectual property (IP) and manufacturing capabilities. This report refers to such efforts as "design-around."

The growing incentive to innovate ways around U.S. export controls has bolstered domestic R&D efforts and potentially placed China on a quicker path toward semiconductor technological superiority in industry segments where it already held strong market share, such as packaging.[29] For instance, advanced packaging innovations offer one potential path for Chinese companies to achieve cutting-edge chip capabilities without needing to replicate Western semiconductor manufacturing equipment technologies.[30]

The growing incentive to innovate ways around U.S. export controls has bolstered domestic R&D efforts and potentially placed China on a quicker path toward semiconductor technological superiority.

Alongside design-out efforts, design-around provides another tool for the Chinese semiconductor ecosystem to reduce reliance on U.S. technologies in supply chains. It also creates potential opportunities for Chinese companies to ultimately *surpass* U.S. technological capabilities in semiconductor supply chains. While testifying to a Senate panel in April 2024, a senior U.S. official dealing with export enforcement called attention to this longer-term danger of the design-around issue. "I'm . . . concerned [about] the day that . . . [the Chinese] don't want our technology, that day that we aren't the world leader, because that means that they've surpassed us and they've become superior."[31]

Impacts on U.S. Economic and National Security

At an elementary level, well-functioning export controls on advanced, dual-use technologies seek to regulate the export of goods when there is no other method of supply. Otherwise, buyers can

simply shift procurement of controlled goods to either domestic suppliers or countries with looser controls. If the controlled technology can be easily sourced from a domestic firm or a foreign country outside of the export control regime (i.e., design-out), then the restriction will only be successful until the replacement technology can fill the resulting demand gap. Additionally, as new substitute technologies emerge (i.e., design-around), export control policies must adjust accordingly, or they risk solely being a hindrance to the home country's export revenue and its influence within the global economy.

During the age of the "sliding scale" approach to export controls, the United States' adversaries consistently lagged behind the technological frontier, in large part due to the global R&D leadership of U.S. companies in key technology areas.[32] In switching to the current approach—"maintaining as large a lead as possible"—the United States hopes to leverage its industry leadership to contain China's technological progression in military and dual-use technologies. However, the design-out phenomenon threatens to unintentionally undermine this goal and ultimately presents a threat, rather than a boost, to U.S. technology leadership over China.[33]

The primary concern with design-out efforts is that they would allow China to divert global semiconductor industry revenue away from U.S. companies, shrinking U.S. market share and creating new opportunities for Chinese and third-country firms.[34] This risk is by no means trivial since the Chinese semiconductor market is—and is expected to remain—the largest in the world.[35] The potential impacts are also not confined to the Chinese semiconductor market itself, as export controls could create new incentives for foreign-based multinationals to limit their use of U.S. technologies to avoid facing export controls that would affect access to the Chinese market.[36]

In this way, current U.S. export controls risk inadvertently allowing foreign companies to supplant U.S. semiconductor champions throughout key parts of the global market. If this happens, U.S. technological companies stand to lose out on the revenue, as well as share price growth, that serves as the feedstock for R&D investment.[37] R&D is critical for companies in the semiconductor industry given the rapid rate of technology change and the importance of maintaining the leading edge, so any reduction in investment can be devastating to a firm's positioning.[38] This means that losses in R&D could entail U.S. companies losing the technology leadership they currently have in key parts of the semiconductor supply chain—the very opposite goal of the export controls.

If China's semiconductor industry can successfully remove U.S. technology from its supply chain, then the U.S. government would also lose access to data on Chinese equipment purchases, which sales from U.S. companies currently provide. This data offers insight into the military and dual-use capabilities available to China's People's Liberation Army (PLA), which confers advantages from a national security perspective. U.S. policymakers would also lose a key point of leverage over China. If China no longer utilizes the U.S. technology to make chips, continued implementation and enforcement of U.S. export controls—as well as the threat of introducing new controls—would do little to advance U.S. economic and national security interests.

Finally, the United States would also give up some of its ability to influence how CETs are developed and utilized, a key advantage within global technology markets. The following table provides an

overview of why CET standard setting is important to U.S. strategic competition with China and other adversaries.

Through this series of reports, the CSIS Scholl Chair will seek to detail and evaluate the design-out and design-around threats as they relate to the Chinese and global semiconductor supply chain. Analysis will focus on four key stages of the semiconductor supply chain. For each stage, findings will highlight (1) the risk of design-out by firms in China and third countries, (2) the potential for design-around solutions, and (3) the effects of these strategies on U.S. economic and national security.

Table 1: U.S. CET Standard Setting

Why are standards important?	Goals of setting standards	U.S. government strategy on standard setting
Standard setting is a critical undertaking that influences the development and usage of new technologies. When strong standards are created and maintained, innovation and technological integrity are bolstered within industries that utilize the standardized technology.[39]	One of the key advantages to being a global first mover for CET development is the ability to set the standards of use. When one set of standards is adopted over another, there are potentially massive benefits for the national economies that utilize the wider-spread set of standards. There is, therefore, an economic and national security imperative for the United States to set the standards of use for CETs. The urgency of standard setting is only heightened when considering China's attempts to set competing technological standards.[40]	In May 2023, the White House released the National Standards Strategy for Critical and Emerging Technologies.[41] Among other things, the strategy document calls for U.S. leadership on CET standard setting, especially as its global leadership is challenged in the twenty-first century.[42]

Source: The White House, United States Government National Standards Strategy for Critical and Emerging Technologies (Washington, DC: The White House, May 2023), https://www.whitehouse.gov/wp-content/uploads/2023/05/US-Gov-National-Standards-Strategy-2023.pdf.

This first report provides a brief introduction to the design-out and design-around phenomena and how they have taken shape within China's government and private sector. It then turns to the packaging segment within semiconductor supply chains, a primary example of the design-around

threat. Advanced packaging represents an area of intensive innovation that China has identified as a strategic priority in efforts to undermine the effectiveness of U.S. export controls.[43]

In subsequent reports, the Scholl Chair will cover the fields of semiconductor manufacturing equipment and tool subsystems and components, as well as electronic design automation (EDA), chip design, and core design IP. Each report will provide evidence for the design-out and design-around phenomena and evaluate the potential impacts of these Chinese counterstrategies. Ultimately, it is argued that the resulting loss of leverage over the global semiconductor industry is detrimental to U.S. economic and national security.

1

China's Evolving Strategy, 2018–Present

The basic motivation behind both design-out and design-around strategies is a recognition by Chinese policymakers and businesses that U.S. (and allies') export controls jeopardize China's critical technology supply chains—and that strategic trade controls are only becoming more common. Such concerns are not new within the highest levels of the Chinese government.[44] Beijing has long been anxious about its reliance on foreign manufacturing for "core technologies," including semiconductors. Xi Jinping's election as general secretary in 2013 led to a strengthening of this focus, reflected in the ambitious semiconductor self-sufficiency goals associated with the landmark industrial policy document "Made in China 2025."[45] Despite these top-down goals, however, Chinese semiconductor companies continued to source key technologies heavily from U.S. and other foreign suppliers.[46]

The Trump administration's 2018 restrictions on ZTE—and their implication that U.S. export controls could put a Chinese national technology champion out of business—created newfound urgency behind efforts to wean off U.S. technology.[47] An additional wake-up call was Huawei's near collapse following its addition to the entity list, which crippled its smartphone business for multiple years.[48] Huawei, alongside Chinese policymakers, made attempts at reshaping domestic technology supply chains to reduce foreign (particularly U.S.) dependencies, investing in new vertical integration efforts and partnerships with local suppliers.[49]

The most important shift, however, came on October 7, 2022. The Biden administration's new rules under the EAR, which were broader than expected by both Chinese and third-country commercial and government stakeholders, fundamentally changed decisionmaking about U.S. technology

within China's semiconductor industry. Almost overnight, Chinese self-sufficiency targets transformed from top-down, broad objectives to an industry-wide supply chain effort to ensure that the future of China's semiconductor industry was safe from current and future U.S. restrictions.[50] As an employee of one top U.S. semiconductor company described it, *"the October 2022 unilateral regulations poured 'jet fuel' on the Chinese innovation economy."*[51]

This series of reports focuses on the key pathways that the Chinese government and businesses have used to pursue this goal of "de-Americanizing" semiconductor supply chains, as well as their consequences for U.S. and global semiconductor markets. In conducting background research, several baseline facts about Chinese semiconductor manufacturing and procurement behavior became apparent:

1. Politics aside, Chinese companies largely prefer to utilize the most advanced semiconductor tools and technologies, most of which are produced in the United States and allied nations. Under normal circumstances (i.e., in the absence of recent export control trends), Chinese firms would likely continue to purchase and utilize U.S. technology in areas where it is industry leading.
2. China is aiming in the long term for a semiconductor manufacturing supply chain free of U.S. equipment. Policymakers and business leaders are directing domestic semiconductor firms to find alternatives to U.S. technology. Government entities are also investing heavily in the domestic semiconductor supply chain through subsidies and R&D programs to create substitutes for foreign technology.
3. There is an ongoing, relatively successful, government-backed campaign across the Chinese semiconductor industry that urges Chinese companies to buy domestic equipment rather than equipment from foreign suppliers.
4. Chinese fabs and other semiconductor industry participants will often purchase Chinese technologies that are less technologically advanced than foreign counterparts in order to reduce foreign dependencies and nurture domestic industry.
5. When there is not a domestically produced substitute to U.S. technology, Chinese firms will look to procure equipment from companies headquartered in countries with less hawkish economic security policies toward China. Buying new equipment from U.S. companies is often seen as a last resort.
6. In response to U.S. export controls, companies from third countries (i.e., not the United States or China) have actively sought to replace U.S. companies in the Chinese semiconductor supply chain. Some have even used the lack of U.S. regulatory impediments as a sales pitch to Chinese customers.[52]

These assertions largely reflect the conclusions of publicly available reporting on China's semiconductor industry. The clearest available evidence in Chinese policy for these trends is "Document 79"—also known as "Delete A," for "Delete America"—a highly sensitive strategic plan to rid Chinese digital supply chains of Western technology that has been partially leaked to Western sources.[53] In the weeks before the landmark October 7, 2022, U.S. export controls package, the

Chinese leadership privately circulated Document 79. The plan, according to reporting from the *Wall Street Journal*, incentivizes firms to procure technology from domestic firms even in cases where foreign alternatives are more advanced.[54]

The trends described in the reports on Document 79 are supported by a wide range of sources. They are also taking place across the semiconductor supply chain, from design to manufacturing equipment to packaging. For instance, in semiconductor manufacturing equipment (SME), Chinese companies such as Advanced Micro-Fabrication Equipment (AMEC) and Naura Technology Group have increasingly won key tenders over U.S. leaders.[55] Within subsystems and components, China is attempting to develop its own extreme ultraviolet lithography (EUV) light sources and replace foreign suppliers for chemicals, gases, and other materials.[56] In design and electronic design automation (EDA), Chinese startups like Moore Threads and Empyrean Technology are beginning to take some share from U.S. companies.[57] These cases are merely illustrative examples out of a broader set of evidence, as these trends will be explored in detail during each supply chain stage's report.

The threat that U.S. companies will be designed-out of key parts of the semiconductor supply chain is multifaceted and growing. Design-out efforts are boosting Chinese companies, as policymakers and businesses are attempting to nurture new domestic alternatives. The efforts are also visible in third-country semiconductor industries, where opportunistic non-U.S. firms are seeking to fill the demand gap in China left by newly shunned U.S. firms.

Design-around threats are also continuing to emerge. Chinese innovation leadership can be seen in several portions of the semiconductor supply chain, some of which are outside the reach of export control regulations. Advanced packaging serves as a key example of this trend, but there are other examples of it in semiconductor manufacturing equipment, such as novel attempts to produce leading-edge chips using older lithography and etching tools.[58]

Current U.S. economic security policy may, therefore, inadvertently cause the very thing it was attempting to prevent: the acceleration of leading-edge semiconductor innovation and manufacturing beyond the boundaries of the United States and its allies.

While this series of reports will cover the Chinese counterstrategies to U.S. export controls in much of the supply chain, this report focuses on advanced packaging. These technologies are a key growth area in chip production today, and they offer a prime case of China's design-around efforts in practice. Importantly, advanced packaging and its associated capital equipment are (1) less technologically challenging to develop—and less exclusively dominated by the United States and its allies—compared to fabrication technologies like EUV lithography and (2) potential enablers of cutting-edge applications such as AI large language models (LLMs) without the need for advanced chips.[59] While design-out efforts are occurring in some parts of advanced packaging, such as a shift away from U.S. packaging tools and inputs like advanced substrates, this paper will focus on design-around because of its greater impact on the industry.

Unsurprisingly, U.S. economic security policymakers seeking to keep China from developing cutting-edge technology feel compelled to counter the enabling power of advanced packaging technologies. However, attempts to broadly control these technologies would likely only serve to damage U.S. companies, which lack dominance in the supply chain and operate in the context of a highly competitive global market. Packaging is a clear example of how design-around threatens U.S. technological superiority and must be addressed appropriately.

Current U.S. economic security policy may, therefore, inadvertently cause the very thing it was attempting to prevent: the acceleration of leading-edge semiconductor innovation and manufacturing beyond the boundaries of the United States and its allies.

This paper focuses only on packaging services and tools.[60] It does not cover packaging design tools and overall chip design services and IP, nor does it cover physical testing tools used during the packaging process. Packaging design and testing will be covered in the briefs on (1) EDA and chip design and (2) semiconductor manufacturing equipment, respectively. Designing advanced packaging relies on many of the same software tools used in chip design, such as Synopsys and Cadence, and often occurs in concert with, or as part of, chip and manufacturing process design by "fabless," or design-only, semiconductor firms and foundries.[61] Testing tools, while used in the packaging process, are also important to semiconductor manufacturing and have more similar design-out and design-around dynamics to semiconductor tools used in areas like etching and process control. For these reasons, these technologies and companies are not covered here.

2

The Rise of Advanced Packaging Technologies

Background: Chasing Moore's Law

Since the infancy of semiconductor technology, chip manufacturers have pursued the twin goals of greater computing power and efficiency. These goals have, for decades, been achieved by increasing the number of transistors on a chip, primarily via component miniaturization. Moore's Law—an observation made by Intel cofounder Gordon Moore in 1965—predicted that the number of transistors that manufacturers could fit onto an integrated circuit would double every two years.[62] Researchers and engineers sought to continually invent ways to put more and more transistors on a chip while optimizing the key tradeoffs between power (P) vs. performance (P) as well as a chip's area (A) vs. its cost (C), a paradigm collectively known as PPAC.[63] For most of the semiconductor industry's history, the winning strategy was continually shrinking transistor sizes. For each successive generation of chip, node names (e.g., "50 nanometers") referred to the actual size of a chip's smallest feature—typically its gate length—which was decreasing rapidly.[64]

However, in recent years, transistor size has been shrinking at a slower rate than in the past, calling into question the durability of Moore's Law and increasing the need for alternative strategies to boost computing power and efficiency.[65] Around the late 2000s, leading-edge node names stopped signifying a chip's exact minimum feature size. Instead, node names began symbolizing total increases in transistor density, which were being enabled less by shrinking transistor sizes than by new methods such as feature depopulation and reductions in space between transistors.[66] However, even these new methods have at times struggled to sustain the pace predicted by Moore's Law in the last decade, and ballooning capital costs to boost transistor density have challenged the economic corollary often associated with Moore's Law, which says that cost per transistor is inversely proportional to the number of transistors.[67]

The Rise of Advanced Packaging

Advanced packaging has emerged as a promising alternative to both boost transistor density and scale processing power and efficiency in other ways—particularly as a more capital-efficient alternative compared to investing in changes at the transistor level.[68] The architectures and materials used to connect different chips to each other and the printed circuit board (PCB) can be as important in optimizing PPAC as transistor architecture itself, representing a key opportunity. For instance, the density of interconnects between memory and logic units within a chip package has historically been a communication bottleneck that has lagged the growth of transistor density.[69]

In previous decades, semiconductor packaging was often regarded as a somewhat commoditized last step in an otherwise highly advanced chip fabrication process. The function of packaging has traditionally been to isolate the chip from other components and keep it connected to the PCB.[70] The PCB, in traditional applications, is responsible for transferring power and information between chips and other circuit components. Conventional packaging is a low-value step in the manufacturing process, and it has historically been outsourced to third-party firms—often located in countries with lower labor costs—that specialize in packaging and testing.[71]

Advanced packaging design, on the other hand, is a newer field seeking to arrange the components of a chip and its interconnecting parts in ways that improve input/output (I/O), reduce latency (the delay period between when a computing instruction is given and when data begins transferring), and increase power efficiency. As such, it incorporates wholly different processes and technologies than traditional packaging.

Notably, advanced packaging occurs during both upstream and downstream manufacturing processes. Traditional packaging is an entirely back-end process, occurring downstream, typically executed by an outsourced semiconductor assembly and test (OSAT) vendor. This outsourcing existed because packaging was lower margin relative to front-end manufacturing due to its commoditized nature, with OSATs competing primarily on cost.[72]

Advanced packaging, on the other hand, is moving much of the packaging process farther upstream.[73] New, innovative methods are changing the way in which foundries prepare chips during fabrication, such as logic and memory fabs collaborating to make their chips integrate seamlessly in the final package.[74] To build advanced packaging architectures, certain technologies and methods need to be integrated throughout the front-end wafer fabrication process, creating opportunities for chip manufacturers to increase their share of industry value-added.

"Chiplets" and Heterogeneous Integration

One particularly important advanced packaging innovation is "chiplet" design, which brings multiple chips with discrete functions into a singular packaged unit. The packaging methods used to bring chiplet designs to life—referred to as heterogeneous integration—have the potential to enable greater power efficiency, faster data transfer rates, and lower signal degradation relative to conventional packaging methods.[75] One major advantage of chiplet design is flexibility in terms of serving different applications. Semiconductor components that interact often in a system can

be placed in greater proximity, reducing latency and power demands. For AI computations, for instance, which rely heavily on memory functions, bringing a memory chiplet closer to the processing core has proven to be a powerful design solution.[76]

Importantly, chiplet technology can be used to create microelectronic systems that perform like those containing leading-edge semiconductors—without any access to the advanced manufacturing technology required to make such chips. Chiplets have therefore become a serious concern for U.S. policymakers seeking to curb the advancement of Chinese technology, as cutting-edge chipmaking tools, such as EUV lithography, represent the key "chokepoints" used to deny China access to advanced semiconductor capabilities.

Imposing Export Controls on Advanced Packaging

To make matters more challenging for U.S. regulators, advanced packaging is, for the most part, enabled by widely available equipment and materials. Unlike semiconductor fabrication, which occurs on the nanometer level (one billionth of a meter) and requires highly sophisticated equipment at every step, advanced packaging processes are typically measured on the micron level (one thousand times larger). While some specialized machinery is required to build advanced-packaged semiconductors, most tools are less technologically niche and challenging to develop in comparison to fabrication. Furthermore, the supply chain for equipment and materials used in advanced packaging involves Chinese companies and has greater supplier diversification compared to SME or chip design, making potential unilateral, bilateral, or trilateral agreements less effective.[77]

There are, however, a couple of hard-to-acquire inputs and technologies that enable advanced packaging and are worth covering specifically: hybrid bonding and advanced substrates. Each of these technologies enables firms to create advanced chip packages that perform well above their traditionally packaged counterparts, even for similar process nodes at the underlying chip level.

HYBRID BONDING

Perhaps the most impactful technology propelling advanced packaging innovation is hybrid bonding.[78] Hybrid bonding, in short, is a method used to vertically connect fabricated semiconductor wafers (commonly referred to as "dies," "die," or "dice" once they are cut into individual chips) using closely spaced copper pads, creating an exceptionally short interconnect distance between discrete chips.[79] Importantly, hybrid bonding enables advanced "3D" stacking of wafers, which is expected to play a key role in future Moore's Law advancements in power and performance.[80] The utilization of hybrid bonding can dramatically increase the performance of a given chip package. Without advancing the process nodes of the underlying semiconductors, computing efficiency can be greatly increased, enabling various leading-edge applications.[81]

Hybrid bonding can be done in one of two ways: wafer-on-wafer (W2W) or die-on-wafer (D2W). In W2W bonding, wafers are stacked on top of one another, and the stack is diced upon finishing. In D2W bonding, wafers are diced into individual chiplets before stacked. Both methods require specialized manufacturing equipment such as die attach and laser dicing tools.[82]

Table 2: Mapping Key Global Players in the Advanced Packaging Supply Chain

Supply Chain Segment	Category	Companies (and Headquarter Countries)
Equipment	Assembly inspection	KLA (U.S.), ASM Pacific (China), ASTI (Singapore), Koh Young Tech (South Korea), Cohu (U.S.), MIRTEC (South Korea), Grand Tec (China)
	Dicing	DISCO (Japan), Accretech (Japan), ASM Pacific (China), Longhill (China), SYNOVA (China)
	Die attaching	Besi (Netherlands), ASM Pacific (China), Fasford Tech (Japan), Canon (Japan), Hoson (China), PROTEC (South Korea), JIAFENG (China), DIAS Automation (China)
	Wire bonding	Kulicke & Soffa (Singapore), ASM Pacific (China), Hesse (Germany), Shinkawa (Japan), JIAFENG (China), DIAS Automation (China)
	Advanced interconnect	ASM Pacific (China), SSP (South Korea), KOSES (South Korea), DIAS Automation (China)
	Packaging	TOWA (Japan), ASM Pacific (China), Besi (Netherlands), HANMI (South Korea), Trinity Tech (China), Grand Tec (China), DIAS Automation (China)
	Integrated assembly	ASM Pacific (China), Grohmann (Germany)
Materials	Lead frames	SH Material (Japan), Mitsui High-Tec (Japan), ASM Pacific (China), Shinko (Japan), Kangqiang (China), Hualong (China), Trinity (China), Yongzhi (China)
	Bond wires	Heraeus (Japan), Tanaka Denshi (Japan), Nippon Micro (Japan), Doublink (China), Kangqiang (China), YesDo (China), KDDX (China)
	Ceramic packages	Amkor (U.S.), Quik-Pak (U.S.), NGK (Japan), Alent (U.K.), Hitachi (Japan), Kyocera (Japan), LG (South Korea), Sumitomo (Japan), BASF (Germany) , Mitsui High-Tec (Japan), Henkel (Germany), Toray (Japan), Tanaka (Japan), Zhongwei (China), Yixing (China)
	Substrates	Ibiden (Japan), NanYa (Taiwan), Shinko (Japan), Samsung (South Korea), Shennan Circuits (China), Zhuhai Yueya (China), AKM (China)
	Encapsulation resins	Sumitomo (Japan), Henkel (Germany), Hitachi (Japan), Sinopaco (China), HHCK (China)
	Die attach materials	Henkel (Germany), Hitachi (Japan), Sumitomo (Japan), Darbond (China), Hysol Huawei (China), Y-Bond (China)

Source: Saif M. Khan, "The Semiconductor Supply Chain," Center for Security and Emerging Technology, January 2021, https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/.

Besi, a Dutch company specializing in tools for advanced packaging, is a major player in hybrid bonding. According to company data, Besi holds 40 percent of the total global market for "die attach" and 74 percent of the total global market for "advanced die placement."[83] Both technologies are critical components of D2W hybrid bonding operations. Besi's major competitors include two Singapore-based companies, ASMPT and Kulicke & Soffa.[84]

Hybrid bonding processes are for the most part executed in fabs rather than OSATs. Key companies developing hybrid bonding capabilities include leading chip manufacturers such as Taiwan Semiconductor Manufacturing Company (TSMC), Samsung, Intel, and SK hynix—as well as Chinese companies such as Semiconductor Manufacturing International Corporation (SMIC) and Yangtze Memory Technologies Corporation (YMTC). But in terms of existing scaled production, hybrid bonding is limited to a handful of AMD chiplets produced by TSMC, and certain 3D memory chips. Key breakthroughs are expected in the next five years, such as TSMC's 3D-stacked system-on-integrated chip (SOIC) packaging, which is expected to reach the market in 2027. This design builds on TSMC's leading chip-on-wafer-on-substrate (CoWoS) process—a "2.5-D" package one step below hybrid bonding in terms of advancement— which has already proven critical for AI data center applications.[85]

ADVANCED SUBSTRATES

A substrate serves two main purposes in the manufacturing and packaging of a chip. First, a substrate is the basic surface on which microfabrication takes place. Second, and more important for the purposes of advanced packaging, a substrate serves as the connecting point between the "brains" and the "electrical highways" of a chip.[86]

The computing operations of a chip occur on the die, in essence the "brains" of the chip. When in operation, information comes in from the printed circuit board (the "electrical highway"), through the substrate, and onto the die, where a computing operation is performed. Then, the processed information leaves the die by passing back through the substrate and returning to the printed circuit board for further transmission.

The expansion of chip capabilities and growth of specialized applications such as 5G infrastructure, aerospace and defense, high-performance computing, and electric vehicles (EVs) increases demand for semiconductors that can withstand high signal frequency, heat, and data throughput requirements. Advanced substrates are often uniquely able to achieve desired high-performance capabilities under these types of conditions. Therefore, chip packages based on advanced substrates such as gallium arsenide (GaAs), gallium nitride (GaN), and silicon carbide (SiC) are growing in importance. The latter two on this list are considered "wide-bandgap" semiconductors, which can operate at higher voltages, temperatures, and frequencies relative to traditional semiconductors and play a key role in the production of various renewable energy technologies.[87]

The current advanced substrate supply chain runs primarily through three geographies: Taiwan, Japan, and South Korea. Combined, companies in these three countries are responsible for 88 percent of global advanced substrate revenues. Taiwan in particular holds a strong share in advanced substrate production, led by companies such as Unimicron, NanYa PCB, and Kinsus. China, however, has ambitions to expand with newer players such as Shennan Circuits and Access. China's growing investment in the advanced substrate market has the potential to shift market share away from the current leaders. The United States, building off government subsidies under the CHIPS and Science Act, also hopes to gain a foothold in the market, although its share remains small.[88]

3

Designing Around U.S. Export Controls via Advanced Packaging

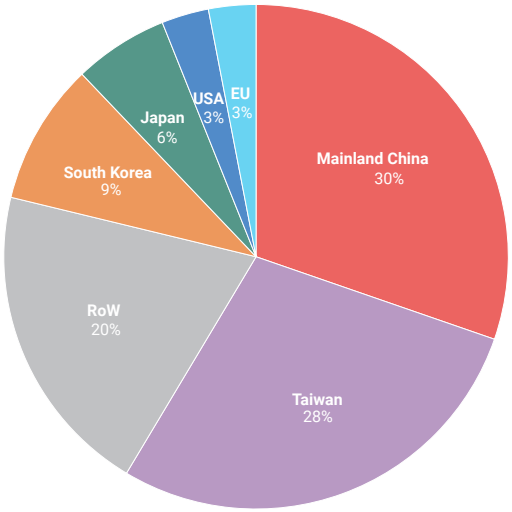
Advanced packaging technologies provide a key opportunity for Chinese government officials and companies to design around U.S. export controls on advanced chips and pursue performance gains via noncontrolled technologies. In these efforts, Chinese companies have a moderate incumbency advantage due to their strong market positioning in conventional semiconductor packaging. While the global packaging market is more geographically distributed than semiconductor industry segments like chip design and fabrication, China is the global leader, controlling 38 percent of total assembly, testing, and packaging (ATP) value-added activity.[89] Key Chinese outsourced semiconductor assembly and test (OSAT) companies include Jiangsu Changjiang Electronics Tech (JCET) and Tongfu Microelectronics, both of which have historically provided low-cost partnerships to key foreign foundries for ATP.[90]

High-volume packaging facilities for U.S. semiconductor manufacturers such as Intel, GlobalFoundries, and Onsemi are located inside China, indicating that packaging technology and expertise are likely widely available in the country. As of 2021, for instance, China was home to 111 ATP facilities for OSATs and 23 facilities for integrated device manufacturers (IDMs), 28 percent of all global facilities (regardless of firm headquarters).[91] Additionally, China holds stronger shares in manufacturing packaging equipment relative to other types of semiconductor tools, giving it some experience with producing required tools such as die attach and bonding.[92]

Leveraging its conventional packaging capacity to build out an advanced packaging ecosystem offers a key opportunity to get around U.S. export controls, and this is indeed what China has begun doing. Chinese OSATs have increasingly pivoted toward advanced back-end processes such as

chiplets over the past few years. In conjunction with its private sector, the Chinese government is also subsidizing advanced packaging research.[93] In August 2023, for example, the Chinese Ministry of Science and Technology announced it would fund up to 30 chiplet-based projects, making over $6.4 million available for research.[94] This is also happening at the local level: in 2023, the city of Wuxi—home to JCET and other Chinese packaging firms—made a pledge to invest $14 million to create a Chinese "Chiplet Valley," a nod to Silicon Valley.[95]

Figure 1: 2022 Industry Value-Added by Country for Assembly, Testing, and Packaging (ATP)



Source: Raj Varadajan et al., *Emerging Resilience in the Semiconductor Supply Chain* (Boston Consulting Group and Semiconductor Industry Association, May 2024), https://web-assets.bcg.com/25/6e/7a123efd40199020ed1b4114be84/emerging-resilience-in-the-semiconductor-supply-chain-r.pdf.

Chinese foundries and chip designers are working to incorporate advanced packaging methods into their semiconductor manufacturing operations. To this end, Huawei, through its subsidiary HiSilicon, has already launched partnerships with packaging equipment vendor JT Automation and wafer probe card startup MaxOne Semiconductor, in addition to securing hundreds of patents.[96] In 2022, Huawei and HiSilicon began innovating with 3D chip stacking designs, an advanced process involving vertical integration of multiple wafer dies into a single package, in an attempt to design around U.S. sanctions.[97] A 2019 patent filing reveals a sophisticated design that makes use of two chips, stacked on top of one another, but only partially overlapping.[98]

SMIC, the most advanced of China's foundries, has called for other Chinese companies to embrace advanced packaging since 2021.[99] SMIC often partners with Huawei to develop chips (including packaging), recently doing so to develop the 7 nanometer (nm) Kirin 9000s for the Huawei Mate 60 Pro smartphone.[100] JCET also recently confirmed its ability to offer packaging capabilities for 5nm

manufacturing processes, linking the OSAT with SMIC's reported efforts to achieve 5nm process production at scale.[101]

YMTC is yet another Chinese entity trying to design around U.S. regulations using advanced packaging. In 2022, YMTC, which is the top Chinese chipmaker for NAND flash memory—a type of semiconductor that stores data without using power, commonly used in memory cards and solid-state drives—employed advanced packaging processes to develop a world-leading memory chip. With different architectures from logic chips, memory chips are measured in the number of layers produced in their manufacturing processes. U.S. export controls prevent the export to China of NAND chips with 128 layers or higher. YMTC's 2022 NAND process produced memory chips with 232 layers, making the firm the first to break the 200-layer milestone.[102] Additionally, the package architecture—called Xtacking—uses hybrid bonding, an advanced packaging process hallmark, demonstrating China's commitment to utilizing packaging as a means of innovation.[103]

Notably, the YMTC 232-layer memory chip attracted the attention of customers beyond the domestic market. In fact, the U.S.-based technology giant Apple planned to use YMTC memory chips in its sold-in-China iPhones in 2022. While the company canceled this plan shortly after the October 2022 U.S. export controls took effect, the episode nonetheless provides an example of the potential global appeal of Chinese advanced packaging technologies.[104] Some analysts have gone as far as to argue that cheaply produced, advanced-packed chips originating from China have serious export potential.[105]

Perhaps the most alarming example of Chinese companies leveraging advanced packaging to design around U.S. controls is the Jasminer X4, a cryptocurrency mining chip that successfully made use of DRAM-to-logic hybrid bonding, a package that involves stacking advanced logic chips on memory chips to boost performance and lower energy demand. While most non-monolithic designs (i.e., packages combining different types of chips) from Chinese companies have been theoretical, the Jasminer X4 is a case of heterogeneous integration in practice. In fact, this is the first demonstrated commercial use of DRAM-to-logic hybrid bonding—a niche heterogeneous integration application that illustrates the ability of Chinese engineers to work around U.S. regulations to manufacture high-performance chips.[106]

The YMTC and Jasminer examples should be a warning sign for regulators in Washington. U.S. export controls, which incentivized the design-around counterstrategy, may well have created a generation of Chinese innovators that seek to push the boundaries of semiconductor technology via advanced packaging. Chinese companies, rather than copying the cutting edge as was seen during the "sliding scale" era of U.S. export control policy, are forced to invent new technologies to design around U.S. regulations. This implicit cultural shift in Chinese commercial goals, from copying to innovation, is a potential sea change in U.S.-China technological competition.

While China has invested heavily into the chiplet ecosystem, it is worth noting that few chiplet designs have been made into physical products, and scaled production remains an obstacle. A key challenge, as with any new semiconductor manufacturing process, will be achieving high yields in production. However, some industry analysts believe that Chinese firms are perhaps just one

to three years away from achieving the wide adoption of heterogeneous integration processes.[107] Chinese companies, including scaled firms and startups, as well as public officials have widely highlighted the promise of advanced packaging—particularly chiplets—as a way around U.S. export controls.[108] One key factor is that the United States does not have significant incumbent advantages in the packaging space, so China is in a strong position to match (or even overtake) U.S. capabilities more quickly.

This implicit cultural shift in Chinese commercial goals, from copying to innovation, is a potential sea change in U.S.-China technological competition.

On a macro level, aggressive U.S. economic security measures—through their impacts on the expansion of Chinese semiconductor innovation—have the potential to harm the very industry leadership they are designed to protect. Chinese advancements in the packaging space present medium- and long-term challenges for U.S. semiconductor companies. Unintentionally, U.S. export restrictions have galvanized Chinese companies to invent novel technologies that threaten the balance of global competition in semiconductor markets.

4

Designing Out U.S. Firms in Advanced Packaging

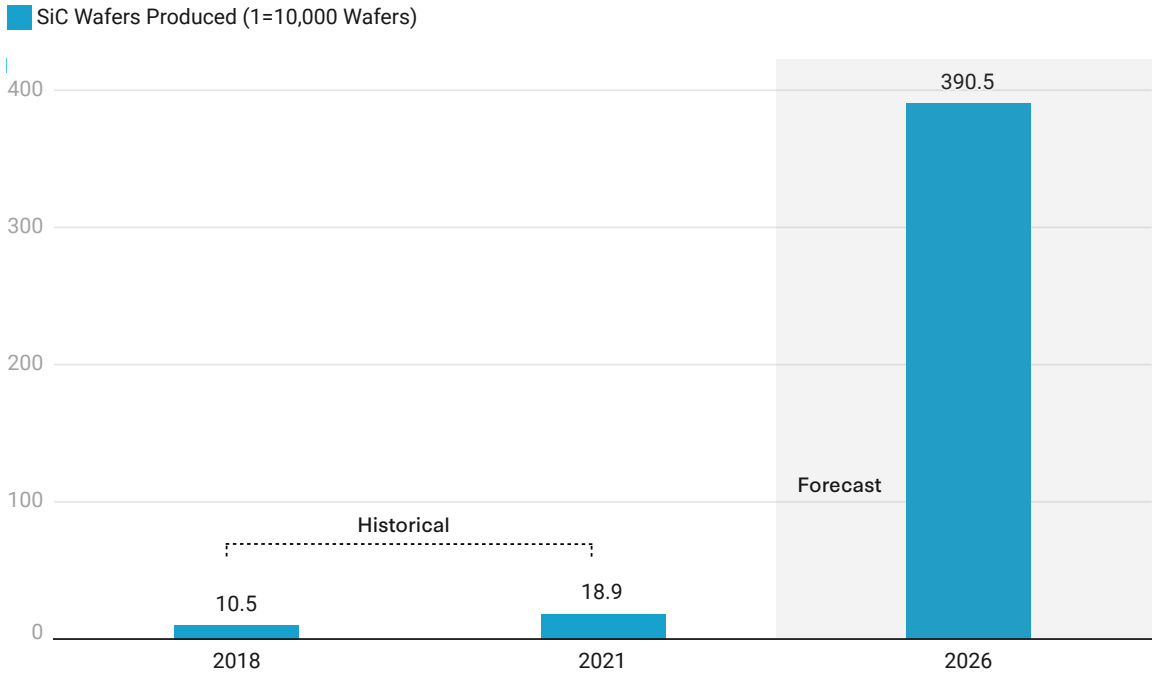
Evidence of U.S. firms being designed-out of the Chinese advanced packaging market is more limited compared to design-around innovations. It requires U.S. companies to occupy leading market share positions in the advanced packaging supply chain, which is less common relative to segments of the semiconductor industry (e.g., tools, design). The strongest example of this taking place is in the advanced substrate market—in particular, silicon carbide (SiC) wafer substrates, which are the foundation of wide-bandgap power electronics semiconductors used in EVs. Despite not being directly affected by the export controls, SiC substrates provide an example of how Chinese decoupling from U.S. semiconductor inputs is affecting technology areas outside of leading-edge chips.

U.S. companies—particularly Wolfspeed and Coherent—along with Japan's SiCrystal, together hold a dominant share of the global SiC wafer market today. North Carolina-based Wolfspeed alone controlled more than 60 percent of the market as of 2021 and pioneered the industry's transition to eight-inch wafers, a key technological breakthrough. SiC-based chips have taken on increased importance within the automotive industry due to their performance benefits compared to silicon wafers in inverters for EVs. China's rapidly growing EV manufacturing capacity represents a key market for SiC wafers for U.S. and third-country firms.[109]

China has targeted expansion in the SiC market for many years (SiC was mentioned in China's 14th Five-Year Plan, indicating plans for government support), but its efforts have recently accelerated.[110] A key focus has been on developing public-private research partnerships with key universities such as the Chinese Academy of Sciences, which has helped China become a leader in SiC patent

filing.[111] At the same time, large private capital investments by EV giants such as BYD and Nio have propelled the growth of emerging Chinese players such as TanKeBlue, SICC, and Sanan. Projections by the semiconductor research firm Yole Group indicate that SiC production within China could see substantial increases in the coming years: 2021 production levels of SiC wafers stood at 0.18 million wafers, whereas 2026 forecasts predict an increase to 3.9 million.

Figure 2: Historical and Planned Chinese SiC Wafer Manufacturing, 2018–2026



Source: AJ Cortese, "That's So SiC: China Aims to Master an EV Chip You Haven't Heard Of," MacroPolo, January 2, 2024, https://macropolo.org/analysis/sic-china-ev-chip/.

While U.S. firms have retained their large leadership so far in terms of SiC market share, the rise of Chinese competitors, facilitated by government support, is expected to create increased challenges going forward.[112] China also has advantages from its leadership in EV manufacturing and integrating SiC-based packages into power electronics systems, providing a strong source of demand and technological knowledge that enables innovative partnerships with domestic SiC substrate suppliers.[113] Overall, this design-out example showcases how China is taking a "whole-of-supply-chain" approach to replacing semiconductor technologies from the United States and its allies, one that has only accelerated following the October 2022 export controls.

5

Summary

The State of Advanced Packaging Today

The semiconductor advanced packaging market is at a critical juncture. While Chinese policymakers and companies are prioritizing packaging innovation and have made key strides, similar efforts are playing out in the United States and around the world. They include increased private sector R&D focused on areas like chiplets and advanced substrates as well as industrial policy investments, such as the CHIPS Act in the United States. As discussed, China has some existing advantages—namely, large domestic conventional packaging capacity and leadership in downstream applications manufacturing for wide-bandgap semiconductors such as EVs and solar panels. That said, China does not hold all the cards in terms of developing advanced packaging, and its long-term leadership in the sector is by no means guaranteed.

Taiwan is currently considered the global leader in advanced packaging, primarily due to TSMC's leading CoWoS product as well as Taiwan's important domestic ecosystem of equipment and packaging materials suppliers.[114] TSMC's capabilities depend on close collaboration in system design with U.S. fabless firms such as Nvidia and AMD (which will be discussed in greater detail in a future paper on design), whose Hopper H200 and Ryzen-16 core packages, respectively, are key market leaders.[115] In terms of OSAT competition, the United States' Amkor and Taiwan's ASE retain the technological edge over China's JCET and Tongfu in terms of advanced packaging.[116] Key OSATs are also increasingly shifting production away from China to geographies like Southeast Asia amid rising U.S.-China tensions.[117]

That said, China's recent progress in advanced packaging should not be taken lightly. There is broad consensus among Chinese and foreign observers that U.S. export restrictions have accelerated

the timeline of innovation in China's advanced packaging ecosystem.[118] Chinese investments into advanced packaging are significant and reflect the high level of government prioritization for the area, which was identified as a Chinese opportunity to surpass the United States even prior to October 2022. Most importantly, the United States and China are working from a similar "starting line" with respect to packaging, unlike most of the rest of the semiconductor ecosystem. The extent to which either country can achieve packaging industry leadership longer term will likely depend closely on effective coordination between a wide range of players, including OSATs, IDMs, designers and EDA firms, foundries, and original equipment manufacturers. In this respect, the increasingly close collaboration across China's entire semiconductor (and electronics manufacturing) ecosystem in response to U.S. controls may present another possible Chinese advantage.[119]

There is broad consensus among Chinese and foreign observers that U.S. export restrictions have accelerated the timeline of innovation in China's advanced packaging ecosystem.

It remains to be seen whether future advancements in the semiconductor industry will be driven primarily by transistor density or changes in systemic complexity such as advanced packaging innovations.[120] Areas such as EUV lithography—access to which is controlled by the United States and its allies—are likely to remain important to PPAC improvements, meaning that the ability of U.S. companies to use these technologies still confers advantages in the overall chip race against China, which is still struggling to develop domestic alternatives. However, the combination of advanced packaging capabilities and advanced fabrication tools represents the most promising way for the United States and its allies to maintain semiconductor leadership. For this reason, the United States cannot afford to let China run away with leadership in advanced packaging, even if it continues to lead in other areas.

6

Conclusion and Policy Recommendations

The United States' new approach to semiconductor export controls attempts to grow its technological lead to the greatest extent possible, rather than simply remaining one step ahead of adversaries. This strategy has produced a range of countermoves from Beijing, including design-out and design-around efforts. Both have the potential to severely impact the U.S. chip ecosystem in the long term. This paper has focused on advanced packaging, which offers China's semiconductor industry a rare opportunity to leverage preexisting advantages in a supply chain segment to avoid using U.S. and allies' chipmaking technologies and leapfrog ahead in innovation.

New export controls focused on advanced packaging technologies, which have reportedly been under consideration, would likely do little to solve this issue due to the previously mentioned challenges of lower industry barriers to entry than chipmaking equipment, a widely distributed global supply chain, and the extent of existing Chinese facilities and know-how.[121] In fact, controls would potentially hurt U.S. industry players seeking to grow in advanced packaging more than they would hobble Chinese competitors. The most effective direct U.S. responses to Chinese packaging advancements therefore likely lie in the "promote" side of economic security rather than "protect."

While the low margins and labor intensity of packaging traditionally made U.S. investment unattractive, these factors are evolving as the value added by advanced packaging increases and plant automation expands.[122] A promising government effort to drive U.S. packaging growth is the National Advanced Packaging Manufacturing Program (NAPMP), a National Institute of Standards and Technology initiative under the CHIPS Act that will invest $1.6 billion in funding

innovation across five packaging R&D areas, including chiplets.[123] Another CSIS paper outlines potential strategies to further boost these efforts, including permitting process changes to develop manufacturing sites, workforce development initiatives, and further public-private partnerships.[124] While increased onshoring of packaging technologies will likely not lead to the United States controlling key chokepoints in the packaging space, it can mitigate the risk of domestic and allied firms being supplanted by superior Chinese packaging technologies. This would also prevent Chinese firms locking in future packaging leadership by leading the global setting of protocol and technology standards in advanced packaging, which will likely shape advanced packaging technology adoption.[125]

China's primary goals—and its already-realized achievements—in advanced packaging are designing around U.S. controls on advanced chips and associated manufacturing equipment. Investments in areas like chiplets may soon enable a range of Chinese electronics systems with processing, power, and cost capabilities that were once only possible using leading-edge lithography tools and inputs—technologies developed and largely controlled by the United States and its allies. The United States, itself not a key leader in packaging, has been unable to meaningfully slow China's rise in the sector.

A potential policy shift on a broader level would be to return to the sliding scale approach to semiconductor export controls. This approach disincentivized countries of concern to invest tremendous amounts of time and money into their own capabilities in attempts to surpass the United States and its allies. Sliding scale strategies kept adversaries behind by letting them consistently access new capabilities—albeit capabilities one or two generations behind the United States. The new U.S. "hard ceiling" approach to export controls incentivizes affected countries and companies to innovate away from their dependencies on U.S. and allied inputs. To be fair, the shift is not quite so clear cut for China. The country has long sought to become more technologically independent—even before the U.S. and its allies tightened their economic security rules. The hard ceiling imposed by export controls over the last two years, however, undeniably brought Chinese efforts to a new scale.

The new U.S. "hard ceiling" approach to export controls incentivizes affected countries and companies to innovate away from their dependencies on U.S. and allied inputs.

A move back to the old sliding scale approach may not be politically feasible, however—and more importantly, it likely would not reverse the damage done to U.S. industry interests. The most notable impact of the current export controls is not China's newfound homegrown capabilities in advanced packaging. Rather, it is the shift in the Chinese industry and government mindset that foreign inputs—particularly U.S. inputs—are no longer reliable because their supply is not secure. The growing U.S. conflation of economic and national security means that leading-edge critical goods are always liable to be controlled, making them less attractive to Chinese buyers.

De-controlling items related to CETs to adjust policy gaps may, therefore, be too little, too late in terms of reversing Chinese design-out and design-around efforts.

This idea that "the ship has sailed" should not be used either as a reason to surrender to Chinese ambitions or as an excuse to expand controls on mature and foundational technologies, such as legacy chips, packaging, or any semiconductor technology with substantial foreign capacity. Such controls would strangle domestic industry, overwhelm BIS capabilities, and exacerbate the Chinese mindset shift related to CETs. Alternative strategies to reduce impacts on U.S. businesses will be discussed in greater detail in a report on semiconductor manufacturing equipment and include greater multilateralization of semiconductor export controls, which may require a narrower focus on certain "chokepoint" technologies and the exclusion of areas such as memory chips.

At the same time, policymakers can redouble efforts to make up for the inevitable losses the U.S. industry will be facing due to design-out and design-around, such as how China's development of advanced packaging may lead to reduced purchases of U.S. capital equipment and chips. These efforts should include, for instance, greater cooperation between the United States and its partners and allies to coordinate state-led investments as well as efforts such as manufacturing expansions and joint R&D projects. These efforts could also include a more ambitious trade policy to ensure that U.S. firms have access to more customers globally, which could help offset lost commercial opportunities within China.

About the Authors

Jack Whitney is a former research intern with the CSIS Scholl Chair in International Business and a strategy consultant in EY-Parthenon's Government & Public Sector. At EY-Parthenon, his work focuses on helping federal government clients understand U.S.-China technology competition, identify vulnerabilities in U.S. critical industry supply chains, and design public-private financing partnerships. Jack's prior work experience includes conducting commercial due diligence for leading private equity funds and corporate strategy assessments for *Fortune* 500 corporations. He holds a BA in philosophy from Williams College.

Matthew Schleich is a former research assistant with the CSIS Scholl Chair in International Business. He currently works as a foreign affairs officer in the U.S. Department of State's Bureau of International Security and Nonproliferation. At CSIS, his research centered around economic security, with a specific focus on developments in U.S. export control policy. He previously worked as a contributing reporter at the World Export Control Review and as an intern for both the Office of the U.S. Trade Representative and the U.S. Department of State. Schleich holds an MA in international relations from Johns Hopkins School of Advanced International Studies and a BA in economics from Gonzaga University.

William Alan Reinsch holds the Scholl Chair in International Business at CSIS. Previously, he was a senior advisor at the law firm of Kelley, Drye & Warren and served for 15 years as president of the National Foreign Trade Council, which represents multinational companies on international trade and tax policy issues. From 2001 to 2016, he concurrently served as a member of the U.S.-China Economic and Security Review Commission. He is also an adjunct assistant professor at

the University of Maryland School of Public Policy, teaching a course in trade policy and politics. Reinsch also served as the under secretary of commerce for export administration during the Clinton administration. Prior to that, he spent 20 years on Capitol Hill, most of them as senior legislative assistant to the late senator John Heinz (R-PA) and subsequently to Senator John D. Rockefeller IV (D-WV). He holds a BA and an MA in international relations from the Johns Hopkins University and the Johns Hopkins School of Advanced International Studies, respectively.

Endnotes

1 Paul Mozur and Ana Swanson, "Chinese Tech Company Blocked from Buying American Components," *New York Times*, April 16, 2018, https://www.nytimes.com/2018/04/16/technology/chinese-tech-company-blocked-from-buying-american-components.html; and Jeb Su, "How the U.S. Export Ban Effectively Bankrupts China's Telecom Giant ZTE: Analysis," *Forbes*, April 17, 2018, https://www.forbes.com/sites/jeanbaptiste/2018/04/17/how-the-u-s-export-ban-effectively-bankrupts-chinas-telecom-giant-zte/.

2 Paul Mozur and Raymond Zhong, "In About-Face on Trade, Trump Vows to Protect ZTE Jobs in China," *New York Times*, May 13, 2018, https://www.nytimes.com/2018/05/13/business/trump-vows-to-save-jobs-at-chinas-zte-lost-after-us-sanctions.html.

3 The White House, "Remarks by National Security Advisor Jake Sullivan at the Special Competitive Studies Project Global Emerging Technologies Summit," September 16, 2022, https://www.whitehouse.gov/briefing-room/speeches-remarks/2022/09/16/remarks-by-national-security-advisor-jake-sullivan-at-the-special-competitive-studies-project-global-emerging-technologies-summit/.

4 Sujai Shivakumar, Charles Wessner, and Thomas Howell, *A Seismic Shift: The New U.S. Semiconductor Export Controls and the Implications for U.S. Firms, Allies, and the Innovation Ecosystem* (Washington, DC: CSIS, November 2022), https://www.csis.org/analysis/seismic-shift-new-us-semiconductor-export-controls-and-implications-us-firms-allies-and#:~:text=%E2%80%98sliding%20scale%E2%80%99%20approach.

5 William Alan Reinsch, Matthew Schleich, and Thibault Denamiel, "Insight into the U.S. Semiconductor Export Controls Update," CSIS, *Critical Questions*, October 20, 2023, https://www.csis.org/analysis/insight-us-semiconductor-export-controls-update.

6 Karen Freifeld, "Exclusive: New US Rule on Foreign Chip Equipment Exports to China to Exempt Some Allies," Reuters, July 31, 2024, https://www.reuters.com/technology/new-us-rule-foreign-chip-equipment-exports-china-exempt-some-allies-sources-say-2024-07-31/.

7 Aadil Brar, "Has China's Huawei Beaten US Chip Controls?" *Newsweek*, October 4, 2023, https://www.newsweek.com/china-us-semiconductor-technology-export-controls-huawei-1831739.

8 Cheng Ting-Fang, "How China's Tech Ambitions Slip through the U.S. Export Control Net," Nikkei Asia, October 20, 2023, https://asia.nikkei.com/Business/Business-Spotlight/How-China-s-tech-ambitions-slip-through-the-U.S.-export-control-net; Ian King and Debby Wu, "Huawei Is Building a Secret Network for Chips, Trade Group Warns," Bloomberg, August 23, 2023, https://www.bloomberg.com/news/articles/2023-08-23/huawei-building-secret-chip-plants-in-china-to-bypass-us-sanctions-group-warns; Dylan Patel, Afzal Ahmad, and Myron Xie, "China AI & Semiconductors Rise: US Sanctions Have Failed," SemiAnalysis, September 12, 2023, https://www.semianalysis.com/p/china-ai-and-semiconductors-rise; and James Titcomb, "China Buys Record Levels of Microchip Kit in Race to Beat Biden Sanctions," *The Telegraph*, January 22, 2024, https://finance.yahoo.com/news/china-stockpiles-40bn-microchip-kit-135319882.html?guccounter=1. Little data is publicly available to corroborate whether Chinese customers of semiconductor technologies are misleading U.S. and allied suppliers about their use of the technologies, but industry analysts have suggested that Semiconductor Manufacturing International Corporation (SMIC) has imported U.S. tools by claiming they were being used in less advanced chip production than they are.

9 Che-Jen Wang, "4 Ways China Gets around US AI Chip Restrictions," The Diplomat, June 28, 2024, https://thediplomat.com/2024/06/4-ways-china-gets-around-us-ai-chip-restrictions/; and Paul Triolo, "A New Era for the Chinese Semiconductor Industry: Beijing Responds to Export Controls," *American Affairs Journal* 8, no. 1 (Spring 2024): 29–52, https://americanaffairsjournal.org/2024/02/a-new-era-for-the-chinese-semiconductor-industry-beijing-responds-to-export-controls/.

10 Paul Triolo, "The Future of China's Semiconductor Industry," *American Affairs Journal* 5, no. 1 (Spring 2021): 90–113, https://americanaffairsjournal.org/2021/02/the-future-of-chinas-semiconductor-industry/.

11 Liza Lin, "China Intensifies Push to 'Delete America' from Its Technology," *Wall Street Journal*, March 7, 2024, https://www.wsj.com/world/china/china-technology-software-delete-america-2b8ea89f.

12 Alex Fang, "Biden: 'We Are in a Competition with China to Win the 21st Century,'" Nikkei Asia, April 29, 2021, https://asia.nikkei.com/Politics/International-relations/Biden-s-Asia-policy/Biden-We-are-in-a-competition-with-China-to-win-the-21st-century.

13 Eduardo Baptista, "China's Xi Calls for Tech Self-Reliance amid U.S. Tension," Reuters, February 22, 2023, https://www.reuters.com/world/china/chinas-xi-calls-technological-self-reliance-amid-tension-with-us-2023-02-22/.

14 Anton Shilov, "China to Give Chipmakers $27 Billion to Counter U.S. Sanctions—Big Fund III Will Have Further Funding Rounds," Tom's Hardware, March 9, 2024, https://www.tomshardware.com/tech-industry/china-to-give-chipmakers-dollar27-billion-to-counter-us-sanctions.

15 Lin, "China Intensifies Push."

16 Mackenzie Hawkins, Ian King, Cagan Koc, and Takashi Mochikuzi, "US Floats Tougher Trade Rules to Rein in China Chip Industry," Bloomberg, July 16, 2024, https://www.bloomberg.com/news/articles/2024-07-17/us-considers-tougher-trade-rules-against-companies-in-chip-crackdown-on-china. The present analysis, which focuses on advanced packaging technologies, will not address examples of companies from third countries filling supply gaps in China that are left by U.S. companies. Research indicates that U.S. firms are not deeply involved in Chinese advanced packaging operations. Therefore, there is not ample evidence to prove that exports from third countries are replacing U.S. advanced packaging technologies in China one-for-one. In subsequent papers in this series, the Scholl Chair addresses areas of the semiconductor supply chain in which U.S. companies are global leaders. In these subsectors—particularly semiconductor manufacturing equipment—there is evidence of U.S. firms being designed-out

of the supply chain and replaced not only by Chinese suppliers, but by opportunistic firms from third countries seeking to fill the demand gap left by the declining U.S. presence in China.

17 Jingyue Hsiao, "Chinese Booming Semiconductor Equipment Market Draws Foreign Companies despite Export Ban," DIGITIMES Asia, November 8, 2023, https://www.digitimes.com/news/a20231108VL205.html; and Monica Chen and Jessie Shen, "Taiwan Fab Toolmakers Secure LTAs from China," DIGITIMES Asia, May 25, 2023, https://www.digitimes.com/news/a20230524PD217/taiwan-mature-process-fab-equipment-china-ic-manufacturing.html.

18 Hideki Tomoshige, "Key Differences Remain between U.S. And Japanese Advanced Semiconductor Export Controls on China," CSIS, *Blog Post*, May 25, 2023, https://www.csis.org/blogs/perspectives-innovation/key-differences-remain-between-us-and-japanese-advanced-semiconductor.

19 Cagan Koc and Takashi Mochizuki, "ASML, Tokyo Electron Dodge New US Chip Export Rules, for Now," Bloomberg Law, July 31, 2024, https://news.bloomberglaw.com/international-trade/asml-tokyo-electron-shielded-from-us-chip-export-rules-for-now.

20 William Alan Reinsch, Thibault Denamiel, and Eric Meyers, *Optimizing Export Controls for Critical and Emerging Technologies: Reviewing Control Lists, Expanded Rules, and Covered Items* (Washington, DC: CSIS, November 2023), https://www.csis.org/analysis/optimizing-export-controls-critical-and-emerging-technologies-reviewing-control-lists.

21 Larry Sussman, "Seagate's $300M Lesson," WireScreen, January 26, 2024, https://wirescreen.ai/blog/fdpr.

22 Lou Xianying, Dai Menghao, Yao Shuang, and Ran Fuyan, "Overview of U.S. New Export Control Rules on Semiconductor," Lexology, November 9, 2022, https://www.lexology.com/library/detail.aspx?g=84c1d0ec-e271-41f6-bf70-f99526994458.

23 Bloomberg News, "Biden Surpasses Trump's Record for Blacklisting Chinese Entities," Bloomberg, April 11, 2024, https://www.bloomberg.com/news/articles/2024-04-12/biden-surpasses-trump-s-record-for-blacklisting-chinese-entities.

24 Larry Sussman, "Regulating A.I. through the Supply Chain," WireScreen, April 10, 2024, https://wirescreen.ai/blog/ai-supply-chain-regulation.

25 Ibid.

26 Ulrike Jasper, "US Export Controls: Update and Help with 'De Minimis,'" AEB, May 27, 2022, https://www.aeb.com/en/magazine/articles/us-export-controls-de-minimis.php.

27 "De minimis Rules and Guidelines," Bureau of Industry and Security, November 5, 2019, https://www.bis.doc.gov/index.php/documents/pdfs/1382-de-minimis-guidance/file.

28 Ibid.

29 Shunsuke Tabeta, "China's SMIC, Chip Sector Boost R&D Spending despite Weak Earnings," Nikkei Asia, September 12, 2023, https://asia.nikkei.com/Business/Tech/Semiconductors/China-s-SMIC-chip-sector-boost-R-D-spending-despite-weak-earnings.

30 Anton Shilov, "Huawei Turns to 3D Chip Stacking, Could Potentially Circumvent US Sanctions," Tom's Hardware, April 21, 2022, https://www.tomshardware.com/news/huawei-patents-stacked-chip-design-method-without-tsvs.

31 Mitt Romney, "Romney Leads Senate Hearing on Strengthening Export Controls Enforcement," transcript, April 10, 2024, https://www.romney.senate.gov/romney-leads-senate-hearing-on-strengthening-export-controls-enforcement/.

32 Shivakumar et al., *A Seismic Shift*.

33 Ibid.

34 Fanny Potkin and Yelin Mo, "Chinese Chip Equipment Makers Grab Market Share as US Tightens Curbs," Reuters, October 18, 2023, https://www.reuters.com/technology/chinese-chip-equipment-makers-grab-market-share-us-tightens-curbs-2023-10-18/; and "Japan's Semiconductor Toolmakers Are Booming," *The Economist,* February 15, 2024, https://www.economist.com/business/2024/02/15/japans-semiconductor-toolmakers-are-booming.

35 Mercy A. Kuo, "The State of China's Semiconductor Industry," The Diplomat, October 2, 2023, https://thediplomat.com/2023/10/the-state-of-chinas-semiconductor-industry/.

36 Matteo Crosignani, Lina Han, Marco Macchiavelli, and André F. Silva, "Geopolitical Risk and Decoupling: Evidence from U.S. Export Controls," *Federal Reserve Bank of New York Staff Reports*, no. 1096, April 2024, https://doi.org/10.59576/sr.1096.

37 Kyriakos Petrakakos, "U.S. Semiconductor Export Controls Might Actually Give China the Edge," The China Project, June 15, 2023, https://thechinaproject.com/2023/06/15/semiconductor-export-controls-a-catalyst-for-chinese-development/.

38 Harald Bauer et al., "Getting Mo(o)re out of Semiconductor R&D," McKinsey & Company, 2011, https://www.mckinsey.com/~/media/mckinsey/dotcom/client_service/semiconductors/pdfs/mosc1rd.ashx; and Kif Leswing, "Intel Used to Dominate the U.S. Chip Industry. Now It's Struggling to Stay Relevant.," NBC News, April 26, 2024, https://www.nbcnews.com/business/business-news/intel-used-dominate-us-chip-industry-now-struggling-stay-relevant-rcna149601.

39 Sujai Shivakumar, *Securing Global Standards for Innovation and Growth* (Washington, DC: CSIS, January 2022), https://www.csis.org/analysis/securing-global-standards-innovation-and-growth.

40 Ibid.

41 The White House, *United States Government National Standards Strategy for Critical and Emerging Technologies* (Washington, DC: The White House, May 2023), https://www.whitehouse.gov/wp-content/uploads/2023/05/US-Gov-National-Standards-Strategy-2023.pdf.

42 Ibid.

43 Jane Lee and Eduardo Baptista, "Chip Wars: How 'Chiplets' Are Emerging as a Core Part of China's Tech Strategy," Reuters, July 13, 2023, https://www.reuters.com/technology/chip-wars-how-chiplets-are-emerging-core-part-chinas-tech-strategy-2023-07-13/.

44 John VerWey, "Chinese Semiconductor Industrial Policy: Past and Present," United States International Trade Commission, *Journal of International Commerce and Economics* 1 (2019): https://www.usitc.gov/publications/332/journals/chinese_semiconductor_industrial_policy_past_and_present_jice_july_2019.pdf.

45 "SIA Whitepaper: Taking Stock of China's Semiconductor Industry," Semiconductor Industry Association, July 2021, https://www.semiconductors.org/wp-content/uploads/2021/07/Taking-Stock-of-China%E2%80%99s-Semiconductor-Industry_final.pdf; and PRC State Council, "Notice of the State Council on the Publication of 'Made in China 2025,'" trans. Center for Security and Emerging Technology, March 10, 2022, https://cset.georgetown.edu/publication/notice-of-the-state-council-on-the-publication-of-made-in-china-2025/.

46 Triolo, "Chinese Semiconductor Industry."

47 Gregory C. Allen, *China's New Strategy for Waging the Microchip Tech War* (Washington, DC: CSIS, May 2023), https://www.csis.org/analysis/chinas-new-strategy-waging-microchip-tech-war#:~:text=In%20April%202018%2C%20the%20United%20States%20dropped%20the.

48 Peter Ellstrom and Allen Wan, "China Secretly Transforms Huawei into Most Powerful Chip War Weapon," Bloomberg, December 1, 2023, https://www.bloomberg.com/graphics/2023-china-huawei-semiconductor/.

49 Liza Lin, Stu Woo, and Raffaele Huang, "The U.S. Wanted to Knock Down Huawei. It's Only Getting Stronger," *Wall Street Journal*, July 29, 2024, https://www.wsj.com/business/telecom/huawei-china-technology-us-sanctions-76462031; and Mackenzie Hawkins, "US Weighs Sanctioning Huawei's Secretive Chinese Chip Network," Bloomberg, March 20, 2024, https://www.bloomberg.com/news/articles/2024-03-20/us-weighs-sanctioning-huawei-s-secretive-chinese-chip-network.

50 Ana Swanson, "Biden Administration Clamps down on China's Access to Chip Technology," *New York Times*, October 7, 2022, https://www.nytimes.com/2022/10/07/business/economy/biden-chip-technology.html; and Triolo, "Chinese Semiconductor Industry."

51 From a CSIS roundtable discussion hosted on July 25, 2024, with semiconductor industry participants and analysts.

52 Informed by author interviews with semiconductor industry experts, March 2024–April 2024.

53 The Reform Bureau of the State-owned Assets Supervision and Administration Commission of the State Council, "Notice on the Initiative to Launch Value Creation Benchmarking against World-Class Enterprises," trans. Center for Security and Emerging Technology, April 8, 2024, https://cset.georgetown.edu/publication/china-document-79-2022/.

54 Lin, "China Intensifies Push."

55 Arjun Kharpal, "China's Chip Equipment Firms See Revenue Surge as Beijing Seeks Semiconductor Self-Reliance," CNBC, September 28, 2023, https://www.cnbc.com/2023/09/28/chinas-chip-firms-see-revenue-surge-as-beijing-seeks-self-reliance.html.

56 Eduardo Jaramillo, "Beijing Wants Its Own EUV Light Source, a Key Part of the Chip Supply Chain," China Project, August 3, 2023, https://thechinaproject.com/2023/08/03/beijing-pushes-china-to-develop-its-own-euv-light-source-a-key-part-of-chip-making-tech/; and Cheng Ting-Fang and Shunsuke Tabeta, "Top China Chipmakers SMIC and CXMT Push to Scrap Foreign Inputs," Nikkei Asia, May 21, 2024, https://asia.nikkei.com/Business/Tech/Semiconductors/Top-China-chipmakers-SMIC-and-CXMT-push-to-scrap-foreign-inputs.

57 Reuters, "China's Moore Threads Valued at $3.4 Bln in Funding before U.S. Curbs—Sources," November 16, 2023, https://www.reuters.com/technology/chinas-moore-threads-valued-34-bln-funding-before-us-curbs-sources-2023-11-16/; John Shiffman and Joshua Schneyer, "US Wants to Contain China's Chip Industry. This Startup Shows It Won't Be Easy," Reuters, December 29, 2023, https://www.reuters.com/technology/us-wants-contain-chinas-chip-industry-this-startup-shows-it-wont-be-easy-2023-12-29/; and Amanda Liang and Judy Lin, "China's Domestic EDA Market Share Doubled, Thanks to Support from 3,451 Local IC Design Firms," DIGITIMES Asia, April 25, 2024, https://www.digitimes.com/news/a20240424PD211.html.

58 Zeyi Yang, "Why China is Betting Big on Chiplets," *MIT Technology Review*, February 6, 2024, https://www.technologyreview.com/2024/02/06/1087804/china-betting-on-chiplets-packaging/.

59 Sujai Shivakumar and Chris Borges, "Advanced Packaging and the Future of Moore's Law," CSIS, *Critical Questions*, June 26, 2023, https://www.csis.org/analysis/advanced-packaging-and-future-moores-law.

60 The back-end stages of semiconductor manufacturing are commonly referred to as assembly, testing, and packaging (ATP). As mentioned, testing is covered within a separate report on semiconductor manufacturing equipment. Assembly and packaging are often used interchangeably, and technologies sometimes grouped under assembly, such as bonding and dicing tools, are often included in discussions of advanced packaging. Due to this overlap, this paper uses the term packaging to refer to both packaging and assembly technology.

61 "Allegro X Advanced Package Designer Platform," Cadence, https://www.cadence.com/en_US/home/tools/ic-package-design-and-analysis/ic-package-design/allegro-x-advanced-designer.html; and Synopsys, "Synopsys and TSMC Accelerate 2.5D/3DIC Designs with Chip-On-Wafer-On-Substrate and Integrated Fan-out Certified Design Flows," press release, August 25, 2020, https://news.synopsys.com/2020-08-25-Synopsys-and-TSMC-Accelerate-2-5D-3DIC-Designs-with-Chip-on-Wafer-on-Substrate-and-Integrated-Fan-Out-Certified-Design-Flows.

62 "Moore's Law," Intel, September 18, 2023, https://www.intel.com/content/www/us/en/newsroom/resources/moores-law.html#gs.5teqzh.

63 Matt Traverso, "A Node by Any Other Name: Transistor Size & Moore's Law," Predict, July 10, 2023, https://medium.com/predict/a-node-by-any-other-name-transistor-size-moores-law-b770a16242e5; and R. Clark et al., "Perspective: New Process Technologies Required for Future Devices and Scaling," *APL Materials* 6, no. 5 (May 29, 2018): 058203, https://doi.org/10.1063/1.5026805.

64 Traverso, "A Node by Any Other Name."

65 By a strict interpretation of this definition, some industry analysts have argued that Moore's Law lost relevance decades ago with the advent of different chip sizes for different applications. However, Moore's Law is today more commonly taken to refer to factors like transistor density, regardless of wafer size. Synopsys founder and executive chair Aart de Geus has used the term the "SysMoore Era" to describe the increasing confluence of Moore's Law transistor count increases with greater systemic complexity (e.g., advanced packaging) to drive performance gains in today's chip industry.

66 Ibid.

67 Audrey Woods, "The Death of Moore's Law: What It Means and What Might Fill the Gap Going Forward," MIT CSAIL Alliances, https://cap.csail.mit.edu/death-moores-law-what-it-means-and-what-might-fill-gap-going-forward; Harald Bauer, Jan Veira, and Florian Weig, "Moore's Law: Repeal or Renewal?," McKinsey & Company, December 2013, https://www.mckinsey.com/~/media/McKinsey/Industries/Semiconductors/Our%20Insights/Moores%20law%20Repeal%20or%20renewal/Moores_law_Repeal_or_renewal.pdf; and David Rotman, "We're Not Prepared for the End of Moore's Law," *MIT Technology Review*, February 24, 2020, https://www.technologyreview.com/2020/02/24/905789/were-not-prepared-for-the-end-of-moores-law/.

68 Joseph Fitzgerald et al., "Advanced Packaging Is Radically Reshaping the Chip Ecosystem," Boston Consulting Group, May 14, 2024, https://www.bcg.com/publications/2024/advanced-packaging-is-reshaping-the-chip-industry.

69 Saif M. Khan, "The Semiconductor Supply Chain," Center for Security and Emerging Technology, January 2021, https://cset.georgetown.edu/publication/the-semiconductor-supply-chain/.

70 Nirmalya Maity, "Heterogeneous Design and Advanced Packaging Enable Advances in PPACtTM Even as Classic Moore's Law Scaling Slows," Applied Materials, September 2, 2021, https://www.appliedmaterials.com/us/en/blog/blog-posts/heterogeneous-design-and-advanced-packaging-enable-advances-in-ppact-even-as-classic-moores-law-scaling-slows.html.

71 Ondrej Burkacky, Taeyoung Kim, and Inji Yeom, "Advanced Chip Packaging: How Manufacturers Can Play to Win," McKinsey & Company, May 24, 2023, https://www.mckinsey.com/industries/semiconductors/our-insights/advanced-chip-packaging-how-manufacturers-can-play-to-win.

72 Ibid.

73 Santosh Kumar, "Advanced Packaging Current Trends & Challenges," Semiconductor Industry Association, September 2020, https://www.semiconductors.org/wp-content/uploads/2020/09/Santosh-Kumar_Yole_Advanced-Packaging-Current-Trends-and-Challenges.pdf.

74 Christian Davies and Qianer Liu, "Why Chipmakers Are Investing Billions into 'Advanced Packaging,'" *Financial Times*, April 24, 2024, https://www.ft.com/content/19710eda-b4c3-488b-a42a-1c6b25c18a12.

75 "All about Chiplet Technology," Cadence, November 29, 2023, https://resources.pcb.cadence.com/blog/2023-all-about-chiplet-technology.

76 Ibid.

77 Khan, "The Semiconductor Supply Chain."

78 "Hybrid Bonding," Applied Materials, https://www.appliedmaterials.com/us/en/semiconductor/markets-and-inflections/heterogeneous-integration/hybrid-bonding.html.

79 Dylan Patel, Myron Xie, and Jeff Koch, "Hybrid Bonding Process Flow—Advanced Packaging Part 5," SemiAnalysis, February 9, 2024, https://www.semianalysis.com/p/hybrid-bonding-process-flow-advanced; and "Hybrid Bonding Basics—What Is Hybrid Bonding?," Brewer Science, July 28, 2022, https://blog.brewerscience.com/what-is-hybrid-bonding.

80 Marko Radosavljevic and Jack Kavalieros, "3D-Stacked CMOS Takes Moore's Law to New Heights," IEEE Spectrum, August 11, 2022, https://spectrum.ieee.org/3d-cmos.

81 "High-End Performance Packaging: 3D/2.5D Integration 2020 Market and Technology Report," Yole Group, November 2020, https://medias.yolegroup.com/uploads/2020/11/YDR20153-High-end-performance-packaging-2020-Sample.pdf.

82 "Supply Chain Explorer: Advanced Chips," Emerging Technology Observatory, last updated October 16, 2022, https://chipexplorer.eto.tech/.

83 "Investor Presentation," Besi, November 2023, https://www.besi.com/fileadmin/data/Investor_Relations/Investor_Presentations/Investor_Presentation_November_2023.pdf.

84 "Who We Are," ASMPT, https://www.asmpt.com/; and "Investor Relations," Kulicke & Soffa, https://investor.kns.com/.

85 Patel et al., "Hybrid Bonding Process Flow"; and Anton Shilov, "TSMC to Expand CoWoS Capacity by 60% Yearly through 2026," AnandTech, May 21, 2024, https://www.anandtech.com/show/21405/tsmc-to-expand-cowos-capacity-by-60-every-year-through-2026.

86 "What Is a Silicon Wafer? What Is It Used For?," WaferPro, January 4, 2024, https://waferpro.com/what-is-a-silicon-wafer/.

87 "Wide Bandgap Semiconductors: Pursuing the Promise," U.S. Department of Energy, April 2013, https://www.energy.gov/eere/amo/articles/wide-bandgap-semiconductors-pursuing-promise.

88 Yik Yee Tan, "Status of Advanced Packaging and IC Substrate," Yole Group, March 8, 2022, https://medias.yolegroup.com/uploads/2023/03/edtm-2023-yg-presentation-slide.pdf; and Bilal Hachemi, "AI Accelerators and HPC: Latest Innovations in the Advanced IC Substrates Market," Yole Group, March 14,

2024, https://www.yolegroup.com/strategy-insights/ai-accelerators-and-hpc-latest-innovations-in-the-advanced-ic-substrates-market/.

89 Jane Lanhee Lee, Ian King, Mackenzie Hawkins, and Jillian Deutsch, "A New Front Is Opening up in the US-China Conflict over Chips," Bloomberg, November 20, 2023, https://www.bloomberg.com/news/features/2023-11-21/tech-war-us-china-competition-moves-into-advanced-chip-packaging; and Raj Varadajan et al., *Emerging Resilience in the Semiconductor Supply Chain* (Boston Consulting Group and Semiconductor Industry Association, May 2024), https://web-assets.bcg.com/25/6e/7a123efd40199020ed1b4114be84/emerging-resilience-in-the-semiconductor-supply-chain-r.pdf.

90 Misha Lu, "AMD Partner, China-Based Packaging Leader Tongfu Micro Reported Q1 2023 Results," DIGITIMES Asia, April 27, 2023, https://www.digitimes.com/news/a20230427VL203/amd-china-osat-tongfu.html.

91 Akhil Thadani and Gregory C. Allen, "Mapping the Semiconductor Supply Chain: The Critical Role of the Indo-Pacific Region," CSIS, *CSIS Briefs*, May 30, 2023, https://www.csis.org/analysis/mapping-semiconductor-supply-chain-critical-role-indo-pacific-region.

92 Emerging Technology Observatory, "Supply Chain Explorer."

93 Lee and Baptista, "Chip Wars."

94 Ben Jiang, "China Funds New 'Chiplet' Tech Research Projects to Advance Semiconductor Goals," *South China Morning Post*, August 3, 2023, https://www.scmp.com/tech/policy/article/3229760/chinas-natural-science-fund-supports-new-chiplet-tech-research-advance-semiconductor-self.

95 Zeyi Yang, "This Chinese City Wants to Be the Silicon Valley of Chiplets," *MIT Technology Review*, February 2024, https://www.technologyreview.com/2024/02/07/1087825/chinese-city-silicon-valley-chiplets/.

96 Julian Ho and Willis Ke, "China OSATs Step up Deployments in Advanced Packaging Field," DIGITIMES Asia, July 8, 2021, https://www.digitimes.com/news/a20210708PD202.html.

97 Shilov, "Huawei Turns to 3D."

98 Che Pan, "Chinese Telecoms Giant Huawei Pushes Semiconductor Packaging Innovation to Ease Disruptions Caused by US Chip Sanctions," *South China Morning Post*, April 7, 2022, https://www.scmp.com/tech/big-tech/article/3173432/chinese-telecoms-giant-huawei-pushes-semiconductor-packaging.

99 Che Pan, "SMIC Urges China to Embrace Advanced Packaging as Moore's Law Slows Nanometre Node Progress and US Sanctions Bite," *South China Morning Post*, January 25, 2021, https://www.scmp.com/tech/big-tech/article/3119174/smic-urges-chinas-chipmakers-embrace-advanced-packaging-moores-law.

100 Matthew Schleich and William Alan Reinsch, "Contextualizing the National Security Concerns over China's Domestically Produced High-End Chip," CSIS, *Critical Questions*, September 26, 2023, https://www.csis.org/analysis/contextualizing-national-security-concerns-over-chinas-domestically-produced-high-end-chip.

101 Anton Shilov, "China Poised to Break 5nm Barrier—Huawei Lists 5nm Processor Presumably Built with SMIC Tech, Defying U.S. Sanctions," Tom's Hardware, December 8, 2023, https://www.tomshardware.com/tech-industry/semiconductors/china-poised-to-break-5nm-barrier-huawei-lists-5nm-processor-presumably-built-with-smic-tech-defying-us-sanctions.

102 Chi Lim Tan, "Comparison: Latest 3D NAND Products from YMTC, Samsung, SK Hynix and Micron," Tech Insights, January 11, 2023, https://www.techinsights.com/blog/comparison-latest-3d-nand-products-ymtc-samsung-sk-hynix-and-micron.

103 Belinda Dube and Simone Bertolazzi, "YMTC 232-Layer 3D NAND Memory: An Unexpected Technological Breakthrough," Yole Group, July 12, 2023, https://www.yolegroup.com/technology-outlook/ymtc-232-layer-3d-nand-memory-an-unexpected-technological-breakthrough-the-chronicles-by-yole-systemplus/.

104 Jaiveer Singh Shekhawat and Akash Sriram, "Apple Freezes Plans to Use China's YMTC Chips—Nikkei," Reuters, October 17, 2022, https://www.reuters.com/technology/apple-freezes-plan-use-chinas-ymtc-chips-nikkei-2022-10-17/.

105 Junko Yoshida, "Chiplets: If It Happens in China, Will It Stay in China?," The Ojo-Yoshida Report, February 15, 2024, https://ojoyoshidareport.com/chiplets-if-it-happens-in-china-will-it-stay-in-china/.

106 TechInsights, "SunLune Jasminer X4 near Memory Etherium Miner with Wafer-To-Wafer Hybrid Bonding Advanced Packaging Essentials," April 2023, https://www.techinsights.com/blog/sunlune-jasminer-x4-near-memory-etherium-miner-wafer-wafer-hybrid-bonding-advanced-packaging.

107 Informed by author interviews with semiconductor industry experts, March 2024–April 2024.

108 Joanna Gao and Judy Lin, "IC Packaging Will Be More Important than Foundry, Says YMTC Chairman," DIGITIMES Asia, July 24, 2024, https://www.digitimes.com/news/a20240723PD215/chairman-semiconductor-industry-yangtze-memory-packaging-tv.html?dt_ref=tag.

109 AJ Cortese, "That's So SiC: China Aims to Master an EV Chip You Haven't Heard Of," MacroPolo, January 2, 2024, https://macropolo.org/analysis/sic-china-ev-chip/; and Poshun Chiu, "Overview of SiC Market and the Supply Chain Evolution," Yole Group, November 10, 2023, https://medias.yolegroup.com/uploads/2023/12/202311-apcscrm_overview-of-sic-market-and-the-supply-chain_pch_external.pdf.

110 Cortese, "That's So SiC."

111 Ibid.

112 Junko Yoshida, "SiC in China: 'Poster Child of the Decoupling Era,'" The Ojo-Yoshida Report, December 7, 2022, https://ojoyoshidareport.com/sic-in-china-poster-child-of-the-decoupling-era/.

113 Cortese, "That's So SiC."

114 Jackson Hu, "Taiwan's Transformation into Global Semiconductor Leadership and Future Challenges," DIGITIMES Asia, February 29, 2024, https://www.digitimes.com/news/a20240225PR200/taiwan-semiconductor-industry-subsidy-tsmc-umc-pure-play-foundry.html.

115 Fitzgerald, "Advanced Packaging."

116 Stewart Randall, "Exploring China's Evolving Role in Advanced Packaging," TechNode, March 1, 2024, https://technode.com/2024/03/01/exploring-chinas-evolving-role-in-advanced-packaging/.

117 Rodney Chan, "Chinese OSATs Gear up for Advanced Packaging," DIGITIMES Asia, June 21, 2024, https://www.digitimes.com/news/a20240620PD220/china-osat-jcet-tfme-advanced-packaging-ic-manufacturing.html.

118 Siu Han and Willis Ke, "3D IC Packaging to Develop Faster under US Trade Sanctions against China, Says AP Memory Chair," DIGITIMES Asia, November 2, 2022, https://www.digitimes.com/news/a20221102PD205.html?fsm=cf2b2419561debce; and Yang, "Why China is Betting Big on Chiplets."

119 Pan, "SMIC Urges China to Embrace Advanced Packaging"; Amanda Liang and Judy Lin, "CSIA Executive Urges China Chip Industry to Forget about Advanced Nodes and Focus on Tangible Victory," DIGITIMES Asia, May 24, 2024, https://www.digitimes.com/news/a20240524PD217/csia-china-semiconductors-chipset-3d-packaging-mature-process.html; and King and Wu, "Huawei Is Building a Secret Network for Chips."

120 Ben Bajarin and Jay Goldberg, "Moore's Law and Process vs. Packaging," The Circuit YouTube channel, January 16, 2023, https://www.youtube.com/watch?v=gRJAd12SogE.

121 Monica Chen, "Next US Export Ban against China Could Target Advanced Packaging," DIGITIMES Asia, September 12, 2023, https://www.digitimes.com/news/a20230911PD221/advanced-packaging-china-huawei-smic.html.

122 John VerWey, "Re-Shoring Advanced Semiconductor Packaging," Center for Security and Emerging Technology, June 2022, https://cset.georgetown.edu/publication/re-shoring-advanced-semiconductor-packaging/.

123 "National Advanced Packaging Manufacturing Program," National Institute of Standards and Technology, February 1, 2024, https://www.nist.gov/chips/research-development-programs/national-advanced-packaging-manufacturing-program.

124 Shivakumar and Borges, "Advanced Packaging."

125 Yang, "Why China is Betting Big on Chiplets."

COVER PHOTO
SAM YEH/AFP VIA GETTY IMAGES

CSIS | CENTER FOR STRATEGIC & INTERNATIONAL STUDIES

1616 Rhode Island Avenue NW
Washington, DC 20036
202 887 0200 | **www.csis.org**