Japan is adopting major new industrial policies with the objective of restoring the international competitiveness of its semiconductor industry. At the end of the 1980s, the industry accounted for over 50 percent of world production—a figure that had fallen to 9 percent by 2022. Today, the Japanese industry lags behind the global technological leaders by an estimated 10 years. Reflecting policymakers’ sense of urgency and concern, Japan has put aside practices that characterized its industrial policy throughout much of the postwar era, including limits on foreign investment and an aversion to allowing major foreign-owned manufacturing facilities to operate in Japan.

Today, collaborations with foreign partners are seen as imperative. On May 4, 2022, at the first meeting of the bilateral Japan-U.S. Commercial and Industrial Partnership (JUCIP), the parties agreed on “Basic Principles on Semiconductor Cooperation,” which outlined a vision for collaborating on objectives and strategies for establishing a more resilient semiconductor supply chain. Then, at the U.S.-Japan summit held on May 23 that same year, a joint task force for developing next-generation semiconductors was launched to implement the Basic Principles. At a meeting of the U.S.-Japan Economic Policy Committee in July 2022, the two countries agreed to pursue joint research and development (R&D) in key technologies, and Japan announced the formation of a public research organization patterned on the U.S. National Semiconductor Technology Center (NSTC) called the Leading-Edge Semiconductor Technology Center (LSTC).

A New Paradigm

While similar-sounding U.S.-Japan accords have been announced over the preceding decades in many sectors—often with little subsequent practical impact—the Economic Policy Committee agreement was concluded against the backdrop of an increasingly assertive China and the recent economic shocks arising out of the Covid-19 pandemic and the disruption of chip supply chains.

Indeed, both governments are approaching their vulnerabilities in semiconductors as a matter of...
urgent priority, with a recognition that neither country can pursue a go-it-alone approach to advanced chipmaking. In both countries, the pandemic has prompted policymakers to focus on the concept of “economic security” and the industrial policies necessary to reduce strategic risk. In May 2022, Japan enacted the Economic Security Promotion Act (ESPA), bundling four separate laws together. The ESPA directed Japanese companies to consider economic security in their decisionmaking.

The result has been a series of dramatic policy measures both in Japan and in the United States—including the enactment of major semiconductor-related industrial promotion legislation, unprecedented bilateral industrial collaborations in chip manufacturing and research, and equally unprecedented restrictions on the export of advanced chip technology to China. Japan's new semiconductor promotional measures roughly correspond to measures the United States is taking pursuant to the CHIPS and Science Act of 2022. Similarly, Japan's recent imposition of new export controls to China on 23 types of chip technology roughly parallels similar trade measures enacted by the United States.

In addition to the bilateral U.S.-Japan accord on Basic Principles, the two countries are participants in the U.S.-East Asia Semiconductor Supply Chain Resilience Working Group (also known as “Fab 4”), a U.S.-led semiconductor alliance that also includes Taiwan and South Korea. Fab 4, which held its first meeting in February 2023, is focusing on how to strengthen the chip supply chain. More broadly, Japan and the United States are also working closely on digital trade issues in the Asia-Pacific region.

The challenge confronting Japan in chipmaking is stark. Japan’s most advanced fabs operate with 40-nanometer (nm) design rules, about 10 years behind world leaders TSMC and Samsung. Japan’s dynamic random-access memory (DRAM) producers, which dominated global markets in the 1980s, have largely exited the business, and the country’s most advanced DRAMs are now made in facilities owned and operated by a U.S. firm, Micron Technology. Japan remains internationally competitive in certain semiconductor device types—such as NAND memory, power semiconductors, microcontrollers, and CMOS image sensors—but as the Japanese government recently acknowledged, the current chip promotion effort may well represent the “last chance” for the country to stake out a strong position in the global chip marketplace.

**Japan’s Emerging Semiconductor Strategy**

In June 2021, Japan’s Ministry of Economy, Trade, and Industry (METI) announced a core strategy for the nation’s semiconductor and digital industries with these elements:

- **Formation of a partnership with the United States.** This enables the design and production of next-generation chips (2 nm and below design rules) by the late 2020s, an objective that is being pursued through the formation of Rapidus, a consortium of Japanese firms in collaboration with IBM and the European research organization IMEC.

- **Development of “game-changing” future semiconductor technologies.** For this purpose, Japan is establishing the LSTC, a government-supported R&D center for advanced chip research. The idea for the LSTC reportedly arose out of the U.S.-Japan discussions that led to the adoption of the Basic Principles. IBM will support the establishment and work of the LSTC.
Establishment of new chip manufacturing bases to make legacy devices. Pursuant to this goal, the government has encouraged the world's most advanced semiconductor manufacturer, Taiwan’s TSMC, to form a joint venture with Japanese firms Sony and Denso (a maker of auto parts): Japan Advanced Semiconductor Manufacturing, which is building a wafer fabrication plant in Kumamoto Prefecture. A second TSMC fab is reportedly under consideration.

Subsidies for domestic chip manufacturing. The Japanese government has indicated that it will subsidize up to one-third of the capital costs incurred by domestic and foreign manufacturers to produce designated types of semiconductor devices (including power devices, microcontrollers, and analog devices), equipment, materials, and raw materials. The subsidies are conditioned on a minimum of 10 years of domestic production, and they will require manufacturers to prioritize domestic shipments at times of global shortage.

Japan’s emphasis on international collaborations represents a major shift for the country, which previously had pursued a policy of achieving self-sufficiency in semiconductors until at least the 1990s. This parallels the United States’ current recognition that regaining leadership in chips is impossible without key foreign partnerships.

Launch of Rapidus
The U.S. partnership prong of METI’s strategy was launched in August 2022 with the formation of Rapidus, a consortium of Japanese companies working in partnership with IBM Research to develop IBM’s 2 nm semiconductor technology for manufacture in one or more fabs to be built in Japan. The first fab, to be constructed in Hokkaido, has a target start-up timeframe of 2026–2027. Rapidus had previously entered into a partnership with Belgium-based IMEC, the foremost microelectronics research organization in Europe, which works with nearly all of the world’s major semiconductor device, equipment, and materials firms.

Rapidus was formed by veteran Japanese semiconductor executives—most notably its president, Koike Atsuyoshi (who recently headed memory maker Western Digital Japan) and its chairman, Higashi Tetsuro (former CEO of chip equipment maker Tokyo Electron). The shares are held by 12 Japanese semiconductor experts. The consortium members are Japanese high-tech and financial firms including Toyota, Sony, NTT, NEC, Kioxia (Toshiba), Softbank, Denso, and Mitsubishi UFJ Bank. Significantly, many of the consortium partners are large consumers of chips; they are expected to constitute an initial market for the output of the consortium. Rapidus is receiving substantial financial support from the government of Japan, reportedly an initial amount of 70 billion yen (about $530 million), most of which will be used to buy two extreme ultraviolet lithography (EUV) machines from ASML of the Netherlands.

Japan remains internationally competitive in certain semiconductor device types . . . but as the Japanese government recently acknowledged, the current chip promotion effort may well represent the “last chance” for the country to stake out a strong position in the global chip marketplace.
In late April 2023, the government announced it would provide an additional 260 billion yen ($1.94 billion) to Rapidus “to bolster the company’s research and development operations.” Rapidus is expected to require about 5 trillion yen ($35.1 billion) in investments to begin mass production.

The U.S. government has also encouraged the formation of Rapidus and the collaboration of IBM with the new entity. Nevertheless, bilateral tensions exist. In March 2023, Orii Yasumitsu, a senior executive at Rapidus, criticized U.S. government export controls on semiconductors as “too aggressive,” the first time a senior executive in the Japanese semiconductor industry has “publicly expressed a negative stance on the US Chips Act.” Orii further said, “U.S. regulations weakened Japan’s semiconductor industry in the past. But now the United States is trying to take back global semiconductor supremacy via regulations again. Korea and Japan must work together to respond to the U.S. moves.”

$LSTC$: The Leading-Edge Semiconductor Technology Center

Japan’s new developmental effort in semiconductors features close collaboration between industry, government, and academia. Thus, the Rapidus effort will be supported by the LSTC, established in December 2022 as an umbrella organization to coordinate Japan’s semiconductor research. The research themes being pursued by the LSTC closely align with the Rapidus workplan. The LSTC will be supported by some of Japan’s existing public research organizations: the National Institute of Advanced Industrial Science and Technology (AIST), Riken (a large scientific research institute largely funded by the government), and the University of Tokyo. The LSTC will be open to researchers from “like-minded” countries.

The LSTC will pursue a number of key themes:

- Establishing leading-edge semiconductor circuit design technology
- Developing leading-edge technology for gate-all-around (GAA) field effect transistors
- Developing mass production technology enabling fast turn-around-time (TAT) between chip design and manufacture
- Establishing 3D packaging technology
- Developing materials for GAA construction and advanced packaging

The LSTC plans to select several dozen students and researchers per year from top Japanese universities for specialized training. Classes will be taught by experts in semiconductor manufacturing and telecommunications technology. Hokkaido, where the Rapidus pilot plant will be located, is to run its own training program.

Aggressive Technological Goals

The Rapidus-IBM-IMEC collaboration is arguably one of the most ambitious in the history of the global semiconductor industry. As noted, Japan is currently 10 years behind world leaders TSMC and Samsung in chip manufacturing technology, operating at the 40 nm node. The consortium proposes to leapfrog multiple intervening nodes in two to three years, to begin production at 2 nm. This would constitute an unparalleled technological feat. Skipping even one node places major demands on a company, such as
increased and more complex design rule checking, additional computation requirements, significantly increased node-over-node IP designer staffing requirements, and numerous evolving techniques that are challenging to implement—all under increased time and cost pressures and while navigating the risk of unanticipated technological unknowns. One analyst writes:

> Think long and hard about skipping nodes . . . There is so much progressive learning node over node now, and the need for this learning does not go away with a node jump. You’ll just end up compressing that learning into the critical path of your next design, while management still expects you to complete that design with the same or shorter schedule as the last one. This can only end in tears.

Rapidus has no experience in manufacturing advanced chips, and to date there is no indication that it will be able to access actual know-how from companies with the requisite experience (i.e., TSMC and Samsung). The key to success may be IBM’s technology, which utilizes GAA transistors or “nanosheet FETs,” which enable device scaling beyond current generation FinFET technology (a form of 3D transistor that allows faster switching times and higher density than planar devices). Multiple nanosheet FETs can be stacked up from the silicon substrate, and they are seen as superior to FinFETs because of their GAA character, reduced size, and higher drive currents. According to one source, “This may be the most disruptive transistor design since the beginning of the integrated circuit.” IBM has also recently announced a breakthrough in interconnect (the wiring between components in a semiconductor) technology, replacing copper as an interconnect material with ruthenium (“Interconnect 3.0”)—which can scale to one nanometer and beyond and still be an effective conductor.

The Rapidus-IBM-IMEC collaboration is arguably one of the most ambitious in the history of the global semiconductor industry. . . The consortium proposes to leapfrog multiple intervening nodes in two to three years, to begin production at 2 nm. This would constitute an unparalleled technological feat.

**Japan’s Chip Infrastructure**

U.S. policymakers and industry leaders are reportedly coming to view Japan as an alternative chip production hub to China, notwithstanding its higher costs. To a significant degree, this perspective reflects Japan’s extraordinary competencies in the tools and materials necessary for the most advanced forms of chipmaking, with Japanese suppliers often representing best-in-the-world in their areas of specialization. These include:

- **EUV lithography**: Japan produces much of that equipment that makes extreme ultra-violet (EUV) lithography use for chipmaking at the advanced nodes possible. Japan’s Tokyo Electron (TEL) has a near 100 percent share of the global market for in-line coaters/developers for EUV, the lithography technique Rapidus will utilize to fabricate 2 nm chips.
• **Chip Stacking:** TEL is also working closely with IBM to enable the world’s first chip stacking operations on 300 mm wafers. TEL has a massive presence at Albany Colleges of Nanoscale Science and Engineering (CNSE) in Albany, New York, sending hundreds of employees to the facility at which IBM conducts much of its applied chipmaking R&D. In March 2023, TEL announced that it would invest $167 million to build a new production facility in northeast Japan, “in anticipation of renewed demand from the semiconductor industry.”

• **Photomasks:** Japanese firms JEOL and NuFlare hold a 91 percent share of the global market for mask-making for EUV lithography.

• **Resist Processing:** Japanese firms TEL and SCREEN hold a 96 percent share of the global market for the equipment needed for resist processing.

• **High-End Photoresist:** Four Japanese companies—Shin-Etsu Chemical, Tokyo Ohka Kogyo, JSR, and Fujifilm Electronic Materials—account for 75 percent of global production of high-end photoresist for advanced chipmaking and hold a near monopoly on the photoresist needed to enable fabrication of devices with EUV lithography. A fifth Japanese company, Sumitomo Chemicals, has recently entered the market for the production of photoresist.

• **Wafer Crystal Machining:** Japanese firms Accretech, Okimoto, Toyo, and Disco have a 95 percent share of the global market for equipment needed for wafer crystal machining. Japanese firms Rorze, Daifuku, and Muratech hold an 88 percent share of the global market for wafer handling equipment.

• **Semiconductor Materials:** Japan is the largest maker of semiconductor materials in the world—a status it has held for decades—holding over a 50 percent share of 14 of the most critical materials needed for chipmaking, including photomasks, photoresist, and silicon wafers.

• **3D Chip Packaging:** Japanese semiconductor materials suppliers, including Nissan Chemical and Showa Denko, are making major new investments to develop and produce materials needed for 3D chip packaging. In 2024, Nissan Chemical will begin mass production of a temporary bonding adhesive used in 3D packaging to keep silicon wafers attached to glass substrates during polishing and stacking, while also allowing removal of the wafers without damage.

• **Silicon Wafers:** Japanese materials firms SUMCO and Shin-Etsu Chemical together hold a 60 percent share of the global market for silicon wafers, essential to chip fabrication.

**Rapidus Work Plan**

Pursuant to the Rapidus-IBM accord, Rapidus is licensing 2 nm technology from IBM; furthermore, as noted, the partners will collaborate at the Albany CNSE to bring 2 nm device technology to production level. At CNSE, IBM is making available an ASML EUV tool—including the requisite specialized air and water handling systems and beneath-the-floor infrastructure—to enable Rapidus engineers to build competency in EUV processes. Rapidus personnel can also benefit from the presence of a constellation of tool and materials firms at the Albany site, including Tokyo Electron, KLA, and Applied Materials. In approximately two years, the Japanese engineers working on 2 nm development at CNSE will return to Japan and set up a pilot line for test runs of 2 nm devices. Rapidus expects to take 2 nm chips to the market by 2027.
Koike said in December 2022 that “it will take several trillions of yen” ($7–15 billion or more) to get pilot production up and running, although he did not indicate where such funds would come from. On April 26, 2023, the government indicated it would give Rapidus 260 billion yen ($1.8 billion) that would be used, in part, to fund the establishment of a pilot production plant at Chitose in Hokkaido. Construction of the plant will begin in September 2023 with a completion target in January 2025, a tight timeframe. Koike is also looking for comprehensive private investment and financing for additional investments in new fabrication plants.

Rapidus will operate as a leading-edge foundry, but it does not seek to compete head-to-head with TSMC and Samsung in making commodity devices at high volumes. Instead, Rapidus will focus on specialized niche technologies that can command a price premium. It anticipates that its strength will be fast turnaround time at which it can deliver specialized devices to specific end users tailored to their needs. Initial production volume is forecast at a modest 50,000 wafers per month. While Rapidus has not disclosed information about its anticipated customer base, its own consortium members are likely to represent a major market for the new foundry’s chips.

On the European side, Rapidus and IMEC have agreed to form a broad strategic partnership. With financial support by METI, Rapidus will become a core member of IMEC’s advanced nanoelectronics program, which receives substantial funding from both the regional Government of Flanders and the European Commission. The partners will focus on key enabling technologies—most notably EUV lithography, which is essential to the fabrication of semiconductors at the 2 nm node. IMEC also enjoys a very close relationship with ASML of the Netherlands, currently the world’s only supplier of EUV equipment. Rapidus has already secured a commitment for ASML EUV tools for its Hokkaido fab.

To facilitate cooperation, Rapidus may send engineers to IMEC for training. IMEC is also reportedly prepared to establish an R&D team in Japan to develop long term R&D roadmaps. Further, IMEC and Rapidus expect to collaborate with Japan’s LSTC, a hub for advanced chip technology development being established by the Japanese government.

**Government Support for U.S. Investors**

The Japanese government’s new promotional effort in semiconductors involves financial support for other U.S.-Japan manufacturing collaborations in Japan. The government is providing 46.5 billion yen ($320 million) to the U.S. firm Micron Technology, which owns and operates production facilities in Japan, to manufacture DRAMs. Micron established a manufacturing presence in Japan in 2012, when it purchased the bankrupt Japanese DRAM maker Elpida Memories. Japanese government funding is reportedly being directed toward the expansion of a Micron fab in Hiroshima to make the company’s new high-capacity low-power 1-beta DRAM, the highest-density DRAM yet produced. U.S. ambassador to Japan Rahm Emmanuel characterized the transaction as an example of how the two countries “are committed to strengthening semiconductor supply chains” and national security jointly.

In 2022, the Japanese government indicated it would provide 92.9 billion yen ($680 million) to a joint venture between Japan’s Kioxia and the U.S. firm Western Digital to manufacture 3D flash memory devices at the joint venture’s production base in Mie Prefecture.
Collaboration with Taiwan

Japan’s new 2 nm chipmaking alliance with IBM and IMEC is paralleled by partnerships with Taiwan’s TSMC to enable the production of legacy chips for use by Japanese industry, along with the development of advanced assembly, test, and packaging technology. TSMC’s presence in Japan is well-established:

- **In 2019**, TSMC established the Japan Design Center in Osaka to develop and refine semiconductor process technologies.

- **In March 2021**, TSMC launched the 3D IC R&D Center in Japan’s Tsukuba Science City, supporting research in advanced semiconductor packaging in collaboration with Japanese companies, public research organizations, and universities. The Japanese government is reportedly supporting this project with 19 billion yen ($150 million), about half of the project cost.

- **In November 2021**, TSMC announced that it would invest over $2 billion in a majority-owned joint venture with Japan’s Sony and Denso to create a semiconductor foundry in Japan’s Kumamoto Prefecture utilizing 12, 16, 20, and 28 nm process technology. The participation of Denso, a major Japanese maker of auto parts, reflects the fact that the Japanese automobile industry has been hamstrung by chip shortages since the onset of the pandemic. Construction began in April 2022 and production is expected to start in December 2024. According to the Nikkei, the Japanese government is subsidizing this effort with an extraordinary total of 476 billion yen ($3.5 billion), perhaps the largest subsidy by the Japanese government to a foreign manufacturer.

- **As of December 2022**, Sony is reportedly setting up a facility near the new fab, from which it will source logic chips to be used to make CMOS image sensors.

- **In February 2023**, TSMC disclosed that it planned to build a second fab in Kumamoto Prefecture—in partnership with Sony and Denso—with an investment of $7 billion, which will utilize 5 and 10 nm process and would start operations in or after 2025. Denso views the new fab’s 10 nm capability as essential to ensuring a stable supply of chips for autonomous vehicles.

A New Focus on the Back End

Japan’s effort to shore up its chipmaking capabilities will include the “back end” of the production process—assembly, test, and in particular packaging, which is seen as playing a crucial role in the development of advanced chips. At present, most back-end operations, including packaging, are located elsewhere due to Japan’s emphasis on international collaborations in China and other countries in Asia. Some key elements of this back-end focus include:

- **Orii Yasumitsu, a senior managing executive officer at Rapidus**, said in December 2022 that “a lot of attention has been focused on the front-end [namely, wafer fabrication,] but we’ll work on the back-end processes as well. . . . We will build integrated front-end and back-end production lines.”

- **Kyocera, a manufacturer of ceramics for semiconductor packaging**, recently announced that it would invest 62 billion yen ($470 million) to build its first new production facility in two decades, which will produce packaging materials for advanced chips.
- **Advantest**, a Japanese maker of chip testing equipment, has **entered into** a technology alliance with Taiwan's TSMC for the developing of testing equipment for high-density back-end applications, which will be implemented at TSMC's 3D IC R&D Center in Tsukuba.

- **Canon**, a leading Japanese maker of lithography equipment, is **introducing** back-end lithography machines that are intended to establish high-density connections between devices to enable improved performance and energy efficiency in a single package.

- **Ulvac**, a Japanese chip equipment maker, is **improving** its equipment for removing microscopic debris, which is being created in greater quantities due to more complex packaging operations. Such impurities can impair chip performance.

- **Sumitomo Bakelite**, a chip materials supplier, is **developing** specialized resin compatible with advanced back-end production processes.

Japan's new promotional effort in semiconductors represents a major departure from the policy characterized by industrial independence that continued at least until the 1990s. Today’s goal is to build a global supply chain in collaboration with the United States and Europe—one which is less vulnerable to shocks such as those which occurred during the pandemic and less dependent on an increasingly assertive China. Similar thinking is driving the semiconductor policies taking shape in the United States and the European Union, opening potentially rich avenues of cooperation. As a METI official put it in August 2022, “The era where the world is at peace and it doesn’t matter who supplies our semiconductors is over.” Japan’s new policies are an ambitious and potentially effective response to this new reality.

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