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Implementing the CHIPS Act

Sematech's Lessons for the National Semiconductor Technology Center

By Charles Wessner and Thomas Howell

The bipartisan CHIPS and Science Act of 2022 **appropriates** federal outlays of $52 billion to increase the domestic supply of semiconductors and encourage the construction and expansion of semiconductor fabrication facilities in the United States. Of this, some $11 billion is directed to research and development (R&D) programs that help ensure foundational technologies in semiconductor manufacturing are researched, developed, and reach scale in the United States. Preeminent among these programs is the National Semiconductor Technology Center (NSTC), envisioned as an enterprise operating in the space between the U.S. research base and existing and planned domestic semiconductor design, manufacturing, and packaging operations.

While the volume of federal aid to the semiconductor industry under the CHIPS and Science Act has no U.S. precedent, federal intervention to shore up chipmakers during a national security crisis has happened before. In the mid-1980s, the government deployed major trade measures and provided significant funding for a research consortium of U.S. chipmakers called Sematech in an effort to reverse erosion of the U.S. industry's competitive position relative to Japan. At that time, policymakers were concerned that the erosion of the U.S. chip industry could compromise the U.S. military's ability to confront numerically superior Warsaw Pact forces.

The call for the NSTC in the CHIPS Act has prompted numerous observers to cite the precedent of Sematech. One defense analyst recently **observed**,

> In 1987, the United States created SEMATECH, . . . a public-private partnership that was designed to direct research on semiconductor manufacturing between major industry players.
>
> Today's situation is reminiscent of the 1980s, when U.S.-based companies were losing ground to global competition due to major investments and subsidies by the Japanese government.

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The question today is whether aspects of that earlier effort—which led to a dramatic turnaround in declining U.S. chip competitiveness—remain relevant today.

Broad Benefits of Sematech

When the industry proposed the consortium, Sematech figured prominently in the debate over whether the United States should or should not embrace "industrial policy." Some believed the U.S. government should not take a direct hand in promoting individual companies or even the semiconductor industry as a whole. Others, including the Department of Defense (DOD) and many leading semiconductor producers, believed a government-industry partnership was needed to counteract the advantages of Japanese conglomerates and government-financed cooperative research programs. After much debate, supporters of a consortium carried the day. The DOD was tasked with **providing $500 million** over five years to be matched by industry contributions. This consortium, called Sematech, brought together industry and government in an industry-led partnership that reduced R&D costs and fostered efficiencies that helped revive the U.S. semiconductor industry and its supply chain.

Drawing on the success of this cooperative partnership model, the CHIPS Act **directs** the creation of the NSTC, a public-private research consortium to serve as "the focal point for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide U.S. leadership in the industries of the future." This consortium is the element of the CHIPS Act that most closely recalls Sematech, though the NSTC, as envisioned, is substantially larger in budget and scope. Like Sematech, the NSTC is likely to be centered on a core facility with research infrastructure and organic staff, linked with a network of affiliated and directly funded regional research centers addressing specific themes. And like Sematech, the NSTC is expected to play a convening role with respect to industry, academic, and government actors in the semiconductor ecosystem as a key aspect of the broader U.S. effort to regain technological parity with global leaders.

As the Department of Commerce implements the CHIPS Act, three broad lessons from the Sematech experience—followed by more operational lessons in designing the NSTC—are worth noting.

- **Coordination through road mapping**. While the semiconductor industry's development of technology road maps predated Sematech, the consortium provided an impetus for developing the International Technology Roadmap for Semiconductors (ITRS)—**in the words** of one chip industry veteran, "Perhaps the best road-mapping effort of all time in any industry." According to former Sematech CEO William Spencer and chief strategy officer Tom Seidel, Sematech itself **was developed** in large part through the road mapping process, engaging key industry players in workshops convened before and during the consortium's first year of existence. The NSTC **can deploy** similar road mapping exercises to direct public and private investment resources toward necessary technology developmental themes according to an agreed timetable.

- **Precompetitive industry cooperation**. One of Sematech's principal achievements was to mitigate long-standing commercial and cultural friction between U.S. chip device makers and their tool and materials suppliers. Recognizing this problem from its inception, Sematech **worked with** equipment suppliers to build consensus on performance targets and then negotiated contracts with the suppliers to build equipment that met those targets, helping suppliers fund R&D for their next generation

of tools. Today, a generation later, device makers and their suppliers have decades of experience working closely together on R&D in venues such as Sematech and the Albany NanoCollege (which eventually absorbed Sematech). Reflecting on this experience, the soon-to-be-formed NSTC is expected to convene the diverse elements of the chipmaking supply chain in research collaborations.

- **Need for robust global supply chains**. The NSTC can also learn from Sematech's failures. Notably, Sematech failed to create a chip supply chain based solely on domestic firms. In perhaps the consortium's biggest failure, a $75 million investment in GCA, a U.S.-based manufacturer of wafer steppers, ended with the company's closure and contemporary critics **charging** that the consortium's fixation on "saving American companies in an increasingly global business is the fundamental problem with Sematech." Absorbing this lesson, the framers of the CHIPS Act have provided for collaboration by U.S. companies with trusted international partners, notably those based in Europe and Japan.

Operational Lessons from Sematech

In addition to these overarching lessons, Sematech's 35 years of experience offer practical advice relevant to today's global competitive landscape.

FLEXIBLE INDUSTRY LED MANAGEMENT

- **Importance of industry leadership**. In creating Sematech, Congress recognized that an industry consortium should be industry led, so it ensured industry direction of Sematech's research program. The consortium's flexible, comparatively simple industry-driven governance structure proved an important aspect of its survival and eventual success.

- **Not-for-profit status**. Sematech **was established** as a not-for-profit Delaware corporation, barred by its charter from engaging in the production of semiconductors for commercial sale. According to Larry Browning and Judy Shetler in ***Sematech: Saving the U.S. Semiconductor Industry***, Sematech's board of directors—drawn from industry participants with the exception of a nonvoting member from the Defense Advanced Research Projects Agency (DARPA)—set general policy and chose the CEO. An executive technical advisory board (ETAB) established broad priorities for R&D and testing while a series of focus technical advisory boards (TABs) advised with respect to specific projects within the ambit set by the ETAB. All ETAB and TAB members were from member companies.

- **Flat management**. The management structure was flat, with only three levels under the office of the chief executive: directors, managers, and project managers.

- **Flexible structure**. Sematech **was directed** by "a central organization, staffed and managed by industry personnel." Research projects were implemented and managed from a dedicated central facility focusing on critical industry needs, though much of the research was conducted off-site in regional Centers of Excellence administered by the Semiconductor Research Corporation, in the laboratories of chip equipment suppliers, or in U.S. National Laboratories. According to Spencer, who headed Sematech from 1990 to 1997, and Peter Grindley in an **article** written five years after Sematech's establishment, "The combination of centralized structure and experienced management gave the consortium the autonomy and flexibility needed to carry through changes in the research agenda as necessary." This ability to change and adapt as needed proved to be a key strength.

INDEPENDENCE FROM GOVERNMENT CONTRACTS

- **Use of grants**. Federal funding of Sematech was provided in the form of grants, not research contracts closely tied to predetermined targets—another source of flexibility. The Federal Office of Naval Research (ONR) administered the grants. DOD procurement contracts typically lock parties into a fixed work program and rigid performance milestones. This is also the case with the structure of contemporaneous European industry-government consortia, which **commonly feature** fixed research agendas managed by government "administrators, often with little direct experience in the industry."

- **Links to DARPA**. Sematech was **loosely supervised** by DARPA pursuant to a memorandum of understanding (MOU). The MOU did not spell out technological objectives or prescribe operational methods but provided only that the consortium develops an annual operating plan in consultation with the secretary of defense and the interagency Advisory Council on Federal Participation in Sematech. This flexible arrangement enabled the consortium to respond to emerging trends and problems in its annual operating plans. DARPA's program manager for Sematech served as a nonvoting member of the Sematech board. DARPA, which had the technical and project management expertise to monitor Sematech's R&D efforts, **did not supervise** operations but "routinely attended management and technical advisory board meetings" in which it made its views known. Sematech was also subject to annual assessments by the General Accounting Office (GAO).

ADAPTIVE RESEARCH OBJECTIVES

Sematech's objectives changed over time to adapt to new circumstances in the semiconductor industry, which Spencer **regards as** "arguably one of its strengths." In the face of rapidly changing industry developments, a contractual relationship with the government with fixed goals and targets years into the future would very likely have resulted in the breakup of the consortium. Sematech made the crucial decision early on to pivot from a consortium primarily focused on horizontal research by device makers to one emphasizing a vertical relationship with suppliers—a major change in direction. Although DARPA voiced some concern over the shift from longer-term research to equipment development, the transition was relatively smooth within the existing governance structure. As some analysts **have observed**, "Sematech's ability to shift its research agenda depended crucially on industry involvement in program management."

Other changes in direction were implemented without major conflicts or litigation with the DOD, or between the consortium's members:

- Sematech management **implemented** significant changes in its handling of intellectual property rights.

- Soon after the inception of the consortium, a planned workforce of 750 was trimmed to 650 to free up funds for more R&D.

- A plan to build new cleanrooms for each projected technology phase was scrapped.

- CEO Robert Noyce decided, with the board's approval, that in 1989 the central fab would be only partially completed, which was adequate for starting up, and that substantial funds would be allocated to off-site projects at companies and the federal laboratories—a hub-and-spoke approach now being advocated for the NSTC.

- According to Shetler and Browning, Sematech's strategic focus **was also expanded** to include the flexible manufacturing of application-specific integrated circuits (ASICs).

FOCUS ON IMPROVING MANUFACTURING PERFORMANCE

While Sematech's initial primary focus necessarily shifted from manufacturing R&D to shoring up an eroding supply chain, it nevertheless introduced and refined numerous practices that enabled members to improve their manufacturing performance by reducing costs, improving quality, and obtaining better yields. While the specific performance-enhancing methods Sematech employed decades ago may or may not be relevant in the current context, they collectively represent timeless best practices, such as brainstorming exercises involving rigorous self-assessment based on data and metrics drawn from actual operating experience, used as a basis to improve manufacturing methods and reduce costs.

- **Sematech's Partnering for Total Quality (PTQ) program**. The PTQ program, for which the consortium budgeted $10 million, **facilitated** the sharing of information with manufacturers and toolmakers on world-class manufacturing practices and cost and financial management.
- **Short-loop testing**. Short-loop testing was a technique used to qualify new semiconductor manufacturing equipment individually instead of integrating it into an end-to-end full manufacturing line (full-loop testing) as originally envisioned when the consortium was launched. Short-loop testing capitalized on advances in computer-aided processes to model and simulate the operation of the tool in a full production line, which turned out to yield equally accurate results 25 percent more quickly than the end-to-end production line method **as described** in Shetler and Browning.
- **Developing industry standards**. One-third of Sematech's clean room space was designated the tool applications process facility (TAPF), dedicated solely to joint development and testing of new chipmaking equipment—a place where device and equipment makers could work side by side and consult on manufacturing goals and equipment needs at the chipmakers' R&D level. Shetler and Browning find that the TAPF **prepared the way** for Sematech's subsequent effort to develop and promulgate broad industry standards.
- **Blind benchmarking**. Blind benchmarking was a practice in which members shared about 50 of their performance metrics on an anonymous basis so that each company could recognize its own data but not that of other members. In one case, a member discovered it was paying more for electricity than any other member and used the data to secure rate reductions from its power vendor. The practice also **served as** a wake-up call for members that discovered their metrics were lagging those of their competitors.
- **Manufacturing Methods Council**. Sematech created an internal council that developed and shared best practices, engaging equipment productivity teams to target the performance of specific tools to identify problems and test solutions. In one case, after a member company found the pumps consumed most of the power a tool used, the productivity team identified which pumps could be idled at given times, working with the toolmaker to adjust idling modes to substantially reduce energy consumption.
- **Troubleshooting**. Sematech ran internal workshops and set up councils to address common challenges, such as finding second sources for spare parts. Prior to Sematech, there was **no forum**

for chip manufacturing personnel in any semiconductor company to "meet, exchange information, and provide consensus technical direction on equipment and materials needs to the supplier community." By the early 1990s, Sematech was convening over 200 such meetings a year focused on chip manufacturing technology, involving personnel from member companies, employees of the federal labs, and university representatives. The information exchanges focused on common manufacturing issues facing the entire semiconductor community.

LEVERAGING INDUSTRY ASSIGNEES

In its early years, Sematech operated with 650–700 employees, of which roughly 220 were assignees from member companies, who typically spent 6 to 30 months working at the consortium. An important aspect of the consortium's success was the fact that many members sent their most talented engineers to Sematech, a difficult sacrifice, particularly for smaller firms. Companies **committed** their best talent in part due to cajoling by Noyce and Spencer as successive CEOs and in part because these companies **wanted** to ensure they fully reaped the technological benefits of their financial contributions to the consortium. Typically, the assignees brought with them their companies' best practices, many of which were incorporated into Sematech's operations.

Sematech assignees facilitated the dissemination and application of research results throughout the U.S. industry. One assignee **recalled**, "If you were assigned in a lithography program, you worked in the lithography program. But you also were responsible to make sure that the lithography companies who were members got the information they needed." The prestige these senior engineers enjoyed in their own companies made them effective internal advocates for the adoption of the technological achievements they had participated in at Sematech.

The assignees also posed challenges for the consortium. Most had technical backgrounds with scant experience in forecasting costs, administering project budgets, or aligning projects with an overall strategic plan. A number brought with them and advocated pet projects from their companies that had little or nothing to do with Sematech's research strategy. To mitigate the problem of these new projects, Shetler and Browning **report** that Sematech established an investment council that "instituted openly understood fiduciary mechanisms and strategic guidelines that reduces [reduced] the detrimental effects of having managers in various areas competing to dominate the contract allocation process."

The NSTC should emulate the productive use of company assignees, subject to appropriate checks and balances, with the caveat that the practice will prove effective only if participating firms contribute top talent. According to **some accounts**, Sematech assignees contributed more to the consortium's research efforts than its organic staff did: "Most of the [Sematech] employees were not in the technical mainstream. Most of the technical mainstream were assignees," suggesting that the success or failure of the NSTC may hinge on the quality of the individuals seconded from member companies.

ESTABLISHING STANDARDS

Establishment of common, accepted standards is essential to the development and deployment of next-generation semiconductor manufacturing technology. Standards are required to enable the interoperability of sophisticated equipment and systems developed by many different companies. Standards make it possible for interested companies to compare, measure, and understand complex tools, materials, and processes.

The National Institute for Standards and Technology (NIST) **observes** that successful standards "are not handed down by the government, but produced through a collaborative process" that ensures collaborators accept and adopt the standards. A retrospective by NIST, which took part in a Sematech project to forge common standards for computer-integrated manufacturing (CIM), found that Sematech played a key role in developing and enabling an industry consensus supporting CIM Framework 1.0, a jointly developed protocol that **allowed** software applications to interact in the same way that Windows-compatible applications interface through the Windows operating system.

- Sematech convened user groups drawn from its member companies to develop CIM specifications.
- Taking the original electronic version of the CIM Framework, the consortium **converted** it to HTML format and posted it online, demonstrating the feasibility of "making the specification available in browsable, electronic form without having to distribute the original electronic document."
- As a member of the information technology (IT) standards organization Object Management Group (OMG), the consortium used CORBA, a protocol promulgated under the auspices of OMG, "as the basis for binding CIM Framework- conformant applications to a computing infrastructure."
- Sematech **contacted** independent suppliers and provided orientation and training with respect to the CIM Framework 1.0 in scheduled classes and public conferences.

Because the NSTC is likely to convene a significant part of the U.S. semiconductor device, equipment, and materials sectors, it will have a potentially important role in facilitating the development, acceptance, and adoption of the new standards required with advances in chip technology.

DEEPENING COLLABORATION WITH FEDERAL LABORATORIES

The U.S. National Laboratories represent a vast pool of expertise and research infrastructure already engaged in advanced research into semiconductor technology, raising the question of how the NSTC can best leverage such ongoing work.

- Sandia National Laboratories in New Mexico has historically pioneered research into semiconductor materials and device physics. Its Center for Compound Semiconductor Science and Technology (CCSST) **features** deep competencies in these themes, as well as state-of-the-art fabrication facilities and advanced device and material characterization laboratories.
- Three U.S. National Laboratories—Sandia, Los Alamos, and Lawrence Livermore—recently **announced** a research collaboration with Intel to develop new memory technologies "to extract orders-of-magnitude performance gains from the basic DRAM [dynamic random-access memory] design itself."
- The NIST is running over 50 research programs in semiconductor-related themes. NIST **operates** two nanofabrication facilities that produce custom microfabricated devices to support its research and measurement efforts.
- The Department of Energy (DOE) has launched the microelectronics Energy Efficiency Scaling for 2 Decades (EES2) initiative, intended to improve the energy efficiency of semiconductor devices a thousandfold over the next two decades. In all, 5 major national laboratories, in addition to DOE's Argonne National Laboratory, and 21 companies and organizations **are engaged** in this effort.

Sematech's successes in deepening productive research ties between federal laboratories and commercial chipmakers remain relevant in the current context. Sematech functioned as a centralized matchmaker between the chip industry and several leading-edge federal labs, notably Sandia, Los Alamos, Oak Ridge, and NIST. These collaborations proved particularly valuable for leading device makers and for smaller equipment makers. Sandia's staff **worked** one-on-one with smaller toolmakers, and its "technical capabilities easily met and often exceeded SEMATECH's needs."

- In 1989, Sematech and Sandia **concluded** a $110 million cooperative research and development agreement (CRADA) that gave U.S. firms access to Sandia's "first-rate facilities and a complete range of science-based expertise" to address specific challenges in thematic areas like tool designs and methodologies and equipment performance and reliability.
- In the same year, Sematech and Sandia **concluded** an agreement to establish the Semiconductor Equipment Technology Center (SETEC) to concentrate the lab's resources on the development of tool designs and methodologies. This led, among other things, to a CRADA to create the Contamination-Free Manufacturing Research Center in 1992 to address defect problems arising from larger die sizes and smaller feature sizes that characterized next-generation semiconductor devices.
- In 1993, Sematech entered into a CRADA with NIST, with Sematech **contributing** $49.4 million and the DOE contributing $53.6 million to address chip manufacturing themes such as materials analysis, equipment and software reliability, and equipment modeling and design.

This partnership approach could offer significant opportunities for the NSTC, which could play a similar intermediary role, identifying areas of expertise and specialized resources at the federal labs and engaging them to address specific technological challenges that arise in its manufacturing R&D activities.

A Word of Caution

While Sematech's successes and potential relevance to implementation of the CHIPS Act have been widely acknowledged, its limitations as a model for the NSTC should be recognized.

- Sematech's initial goals were precisely defined and narrow: to achieve world leadership in the manufacture of 0.35-micron silicon-based complementary metal-oxide semiconductor (CMOS) devices by 1993 using U.S. tools and materials. Sematech did not address themes such as computer-aided design, silicon materials, packaging, testing, and other key aspects of semiconductor manufacturing. At present, the NSTC's mandate and goals are far more comprehensive and the technologies involved less homogeneous—factors that may complicate the effort to achieve consensus among the actors with respect to research themes, resource allocation, and ultimate objectives.
- Despite broad agreement on initial goals, Sematech's first years were characterized by major internal conflicts arising out of cultural clashes between participating firms with divergent goals and friction with supply chain firms. Three of the original 14 consortium members **pulled out**. While internal differences were partially ironed out over time, there is no guarantee of a similar outcome with respect to powerful centrifugal forces that could affect the operations of the NSTC. Effective, credible management and sharing of resources to include the needs of smaller companies and start-ups will be essential.

Assessing Sematech's Accomplishments

Virtually from its inception, critics proclaimed Sematech a failure, almost as an article of faith. This ideological presumption has continued to the present day, with one commentator **stating** in August 2022 that "U.S. government efforts to revitalize the nation's semiconductor industry, such as SEMATECH, failed miserably." If this perspective is accurate, use of any aspect of Sematech's experience as a model for implementation of the CHIPS Act would be problematic. Yet the evidence—which comes directly from firms that participated in Sematech—does not support these claims.

In fact, Sematech is generally recognized today as having played a central role in U.S. firms' efforts to recapture global competitive leadership from Japanese chipmakers in the 1990s, which was its core objective. As one comprehensive analysis observed, the participating companies made substantial financial contributions to establish the consortium, and they continued contributing their own resources long after federal support ended. Their actions suggest these firms saw a clear value proposition even after the withdrawal of federal funds, collectively **regarding it** as "a privately productive and worthwhile activity." The member firms consistently committed top talent to the consortium, a practice that would have been reversed had the effort been perceived as a failure. Ironically, the foreign competitors may have had a clearer, less ideological view, with the Japanese chip manufacturers viewing Sematech as a major force underpinning the U.S. chipmaking revival and **prompting them** to support the formation of a new generation of Japanese research consortia patterned on Sematech.

Sematech's principal achievement was an ambitious one—rallying a U.S. chip industry that was on the verge of collapse. But some concrete performance metrics exist:

- **Market share**. In 1988, U.S. chipmakers **trailed** their Japanese rivals in both quality and market share, controlling 43 percent versus 46 percent of the world semiconductor market. But by the early 1990s—a time frame virtually entirely coextensive with Sematech's first five years of operations—those positions had reversed. By 1992 U.S. semiconductor equipment makers reached market share parity with Japan, and by 1994 the U.S. semiconductor device global market share had reached 48 percent versus 36 percent for Japan.
- **Improved yield**. According to the consultancy VLSI Research, Sematech-driven equipment improvements **enabled** U.S. chipmakers to cut the Japanese industry's yield advantage from 50 percent in 1985 to 9 percent in 1991.
- **Lower-cost R&D**. Prior to Sematech, U.S. producers **had to increase** R&D outlays by 30 percent for each new chip generation, whereas soon after the advent of Sematech, the figure fell to 12.5 percent and continued to drop into the single digits.
- **Shorter cycles**. Sematech **enabled** the U.S. industry to compress miniaturization cycles from three years to two, accelerating innovation for a decade and a half and setting U.S. chipmakers on track to overtake their Japanese competitors. The shorter cycles appeared to **lengthen substantially** in 2014 and beyond with the advent of the 14-nanometer node.
- **Higher R&D returns**. By the early 2000s, Sematech members were reporting an annual return on their R&D investments of 20 to 1. As one participant **remarked**, "This is what happens . . . when

seeming competitors pool their resources. This has brought more than $2 billion in research value to members over five years."

Critical Role of Sustained Public Funding

Despite its success, the lack of government support after 1993 proved to be a long-term weakness for the consortium. The initial result of the end of federal funding was a downsizing of the consortium, which was only partially counteracted by inviting foreign firms to participate. This enhanced international cooperation but involved less focus on the needs of U.S. industry and did not allow for the level of investment needed to keep the organization vibrant.

This factor in the evolution of Sematech is significant and offers an important lesson for the NSTC. Similar organizations such as the Interuniversity Microelectronics Centre (IMEC) in Belgium have prospered over time, in no small part due to sustained and substantial public funding, still at **25 percent** of a much-increased budget—after 40 years of operation. A potentially fatal weakness of the CHIPS Act provisions for the NSTC is the idea that in five years, it will be self-sustaining. This is most unlikely and is rebutted by the sustained public support that has underpinned successful consortia such as IMEC, the German Fraunhofer system, and research institutes such as Taiwan's Industrial Technology Research Institute (ITRI). Continued public support will be essential for the ultimate success of the NSTC.

Broad Trade Policy Support

The U.S. government undertook trade negotiations in 1985–86 pursuant to **Section 301 of the Trade Act of 1974** to stop dumping by Japanese producers, which had threatened to put much of the U.S. industry out of business or simply reduce its revenue to the point businesses would be unable to make the investments necessary to compete. The 301 negotiations were flanked by antidumping proceedings in DRAMs and erasable programmable read-only memory (EPROMs), two important commodity memory device types.

The Semiconductor Trade Agreement of 1986 was remarkable in that it did not stop Japanese-produced semiconductors from entering the United States, but it did stop their dumping in the U.S. market and in third countries. Initially, the higher prices **resulted in** a revenue bonanza for Japanese producers, but they also enabled the U.S. industry to compete on quality as well as price. The agreement also required the closed Japanese market to be opened, which occurred in a phased manner during the 1990s. The trade agreement allowed U.S. firms to invest and prosper, while some evolved to newer technologies such as microprocessors. The revived U.S. device industry had a correspondingly positive effect on U.S. equipment providers, which in turn furnished emerging Korean producers with cutting-edge equipment, thereby contributing to a more competitive global semiconductor market.

A key factor in the success of the 1986 trade agreement, after Japanese violations of several previous agreements, was the willingness of the administration under U.S. president Ronald Reagan to impose sanctions on the Japanese industry, targeting imports of Japanese end products incorporating semiconductors rather than the chips themselves. This was a powerful signal to the Japanese government, one that ensured enforcement of the Semiconductor Trade Agreement and thus the continued viability of U.S. producers. The government commitment may also have been a positive signal for the capital markets' view of the industry, a demonstration that the government was not prepared to see the industry crippled by Japanese trade practices.

Sematech's success should be seen in the context of this broader policy response. The recovery and subsequent growth of the U.S. industry was a combination of cooperative technology development, effective trade policy, and the ability of U.S. companies to invest and innovate. The recovery might be likened to a three-legged stool: questions as to which leg matters most are pointless; all three must work together. ■

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